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Low damage integration of ultralow-k porous organosilicate glasses by Pore-Stuffing approach

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Outline

i. **Cu/low-k interconnect and plasma induced damage**

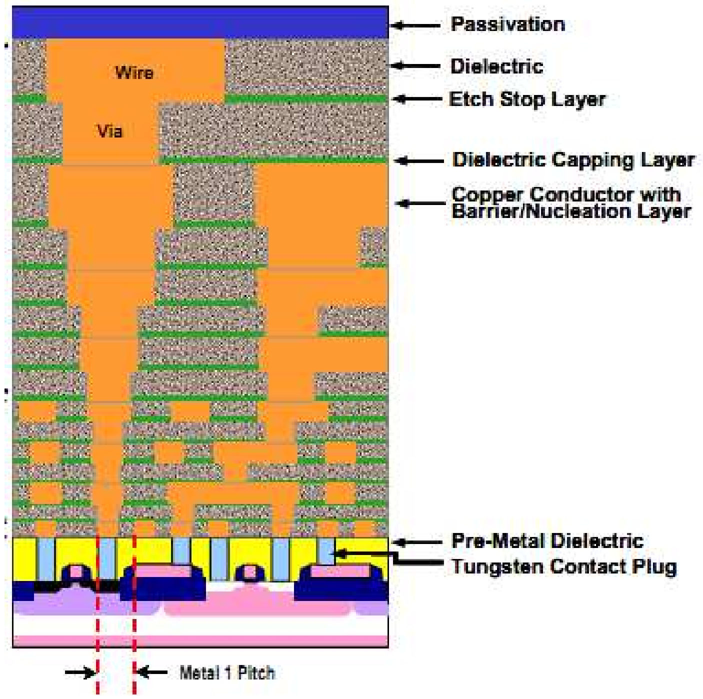
ii. **Pore stuffing - Process flow**

iii. **Plasma Induced Damage**

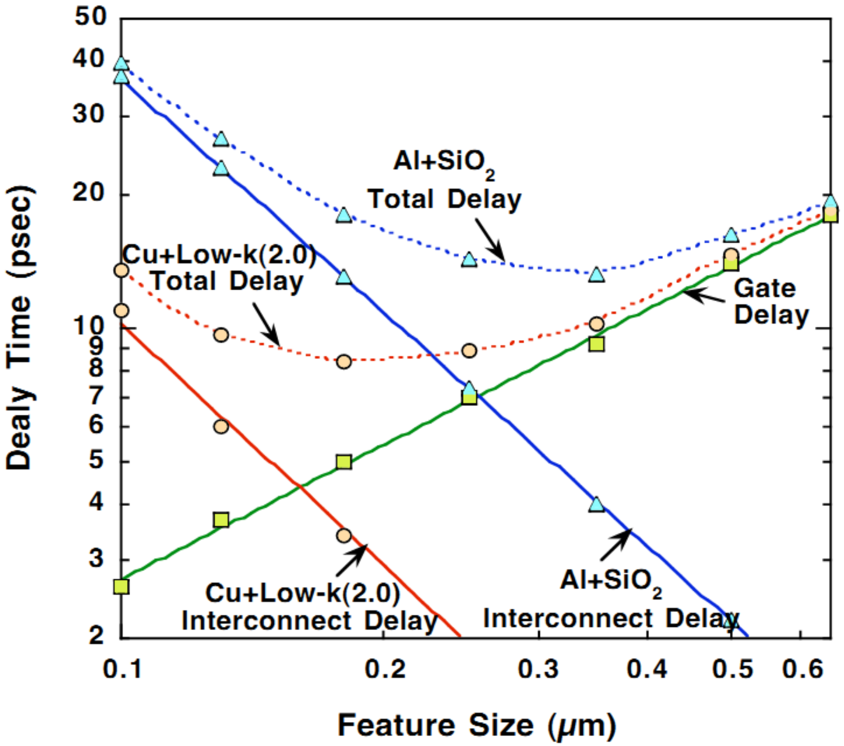
iv. **Integration flow with Pore Stuffing**

v. **Summary**

Cu/low-k interconnect



ITRS, 2011



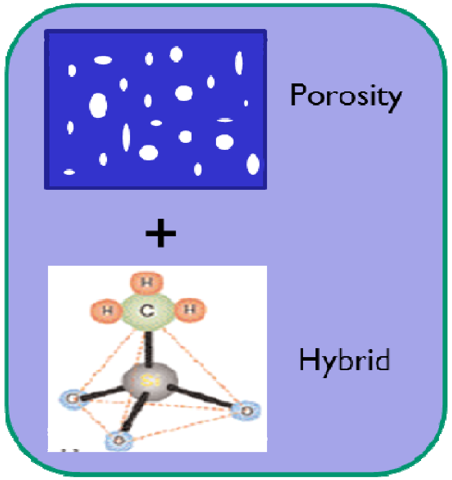
- **Interconnect RC delay will dominate the total time delay as IC scales down.**

$$RC \approx 2 \cdot \rho \cdot \kappa \cdot \varepsilon_0 \cdot L^2 \left(\frac{1}{W^2} + \frac{1}{T^2} \right)$$

Al	→ Cu	SiO_2	→ Low-k
3.0	→ 1.72×10^{-8} Ωm	4.2	→ 3.7-1.8

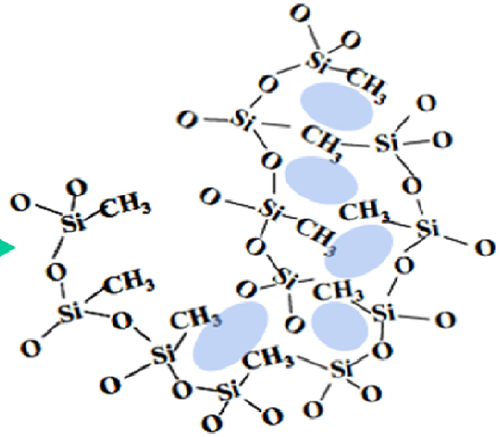
- **Cu/low-k interconnect was introduced to replace Al/SiO_2.**

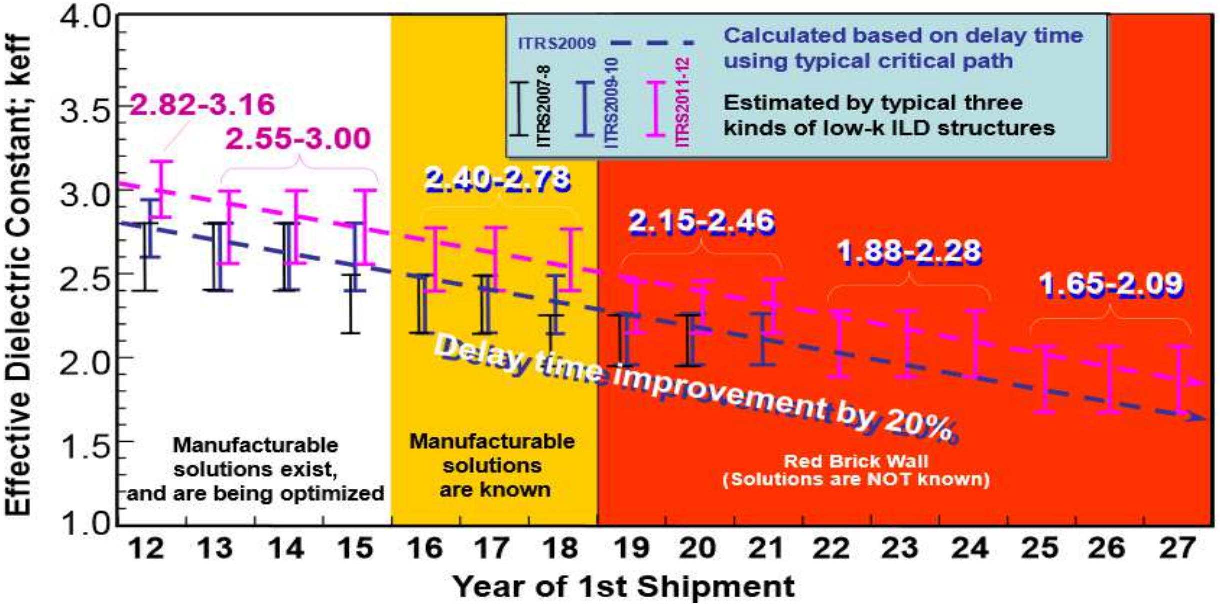
Porous OSGs



$$\frac{\varepsilon_r - 1}{\varepsilon_r + 2} = \frac{N}{3\varepsilon_0}\left(\alpha_e + \alpha_d + \frac{\mu^2}{3kT}\right)$$

PECVD
Spin-coating





- **High porosity**
- **Large pore size**

⬇

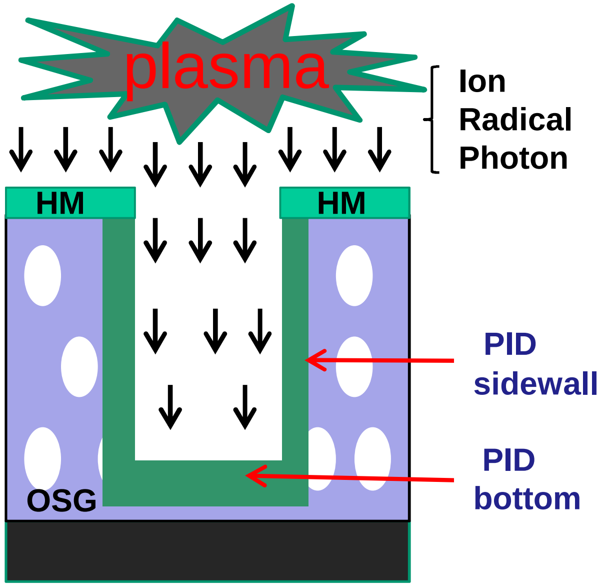
- **Low plasma resistance**
- **Low mechanical strength**

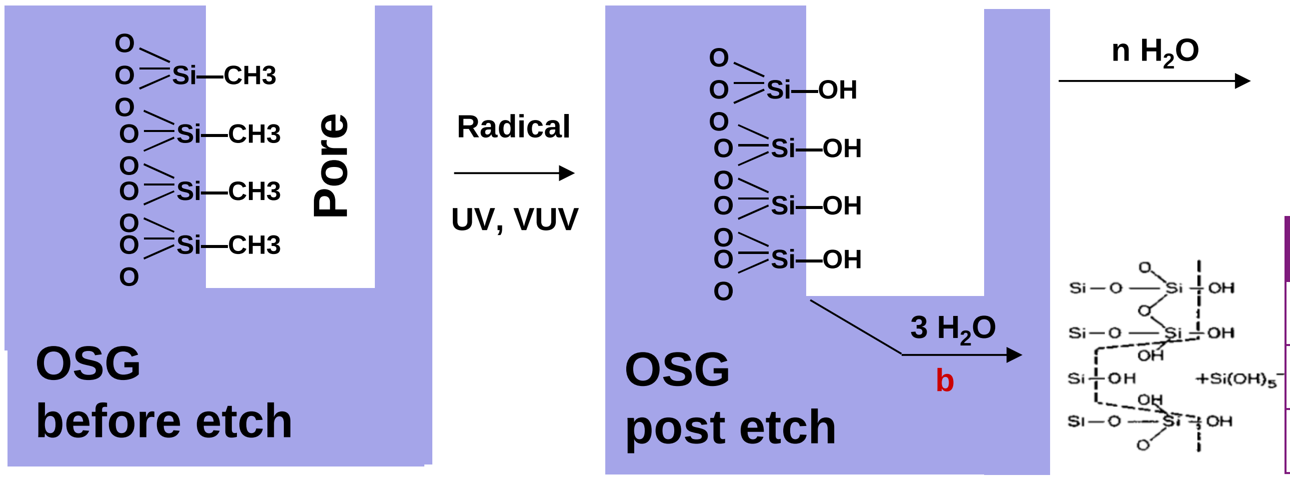
- **Solutions are not known for sub2.2 low-k dielectrics.**

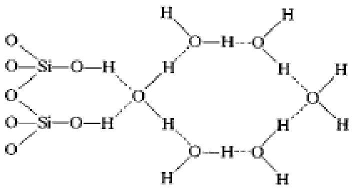
Plasma Induced Damage (PID)

- **Plasma process is widely used in BEOL, for example: Deposition, Cleaning and Patterning.**
- **Depth of damage increases with porosity and pore size: L~ a*d*$N^{0.5}$ (Random Walk Theory).**

  N = <number> of collisions before recombination; d = pore diameter; a = distance for a jump; L = depth of penetration.
- **Reducing PID is a crucial challenge for porous OSG integration.**



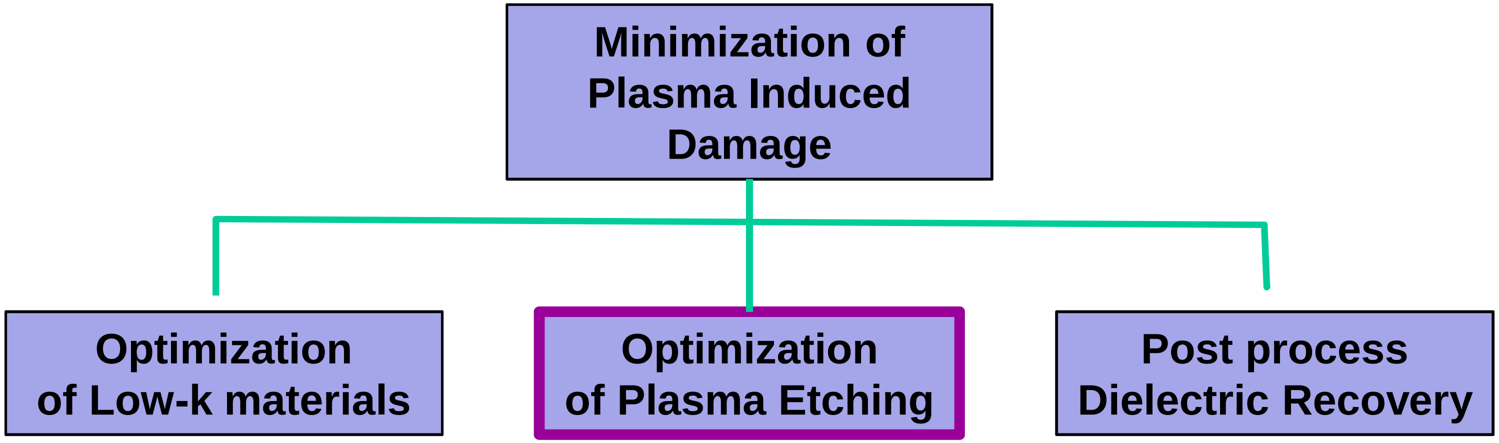




Material	K-value
SiO2	3.8
Low-k	1.8-2.4
Water	79

Moisture uptake leads to increasing of k-value & leakage current

Advanced low-k integration



Minimization of Plasma Induced Damage

Optimization of Low-k materials

Optimization of Plasma Etching

Post process Dielectric Recovery

- Engineering of the chemical composition and porous structure.
- Optimization of plasma species or integration process, Post-plasma porogen removal.
- Restoring the methyl groups by CH_4 plasma or silylation agents, eliminating -OH bonds and physisorbed water by UV irradiation.

→ These approaches are limited and/or complex. New approach is needed.

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i. Cu/low-k interconnect and plasma induced damage

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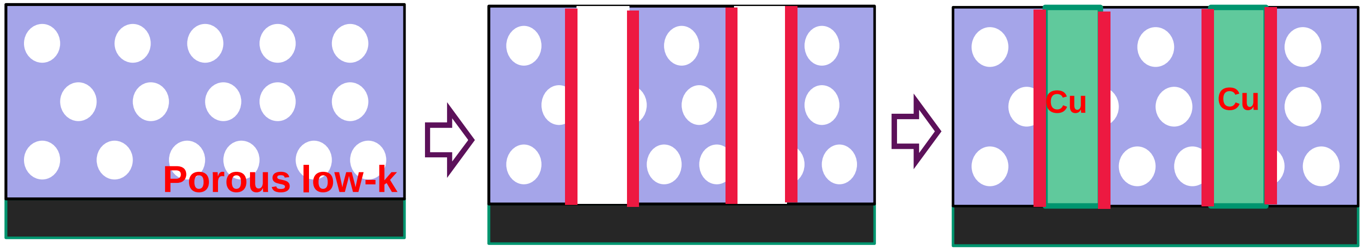
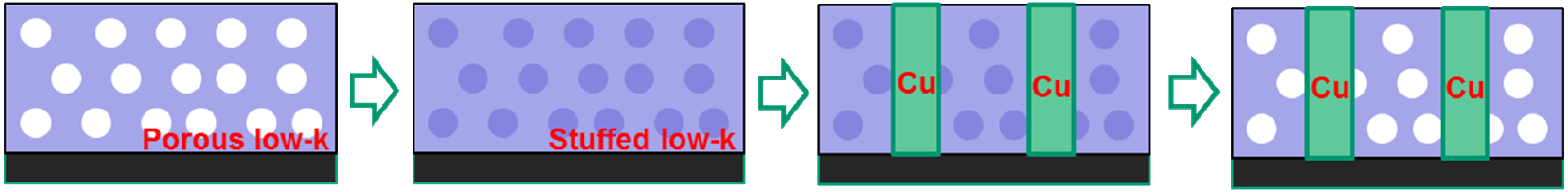
v. Summary

Damascene integration with Pore-Stuffing



- Conventional Cu/low-k integration flow.
- Damage caused by plasma etching + TaNTa barrier penetration degrades k_{eff}.



1st step
Deposition low k
Porous Organic Silica

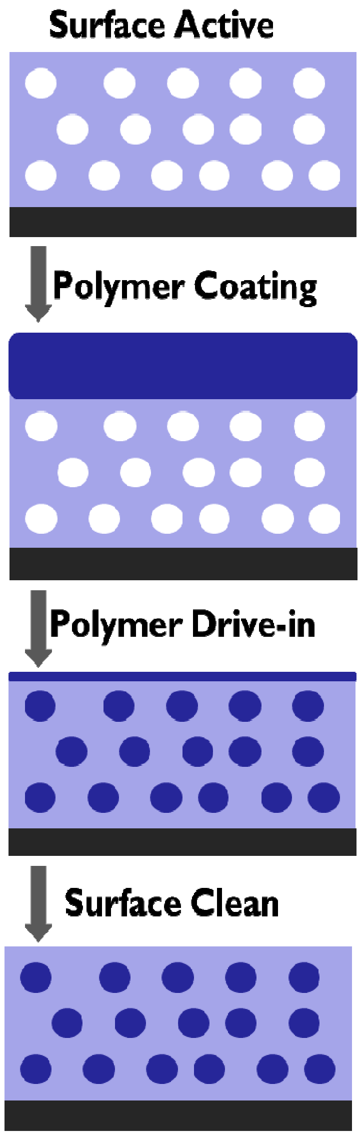
2nd step
Pore stuffing
Thermal drive-in

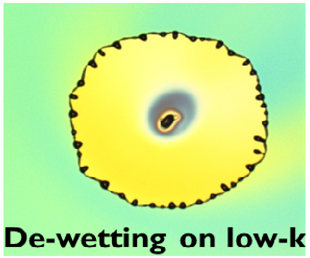
3rd step
Patterning
Metallization, CMP

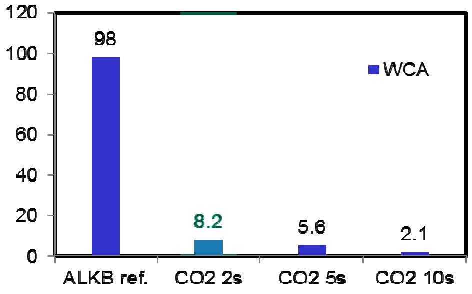
4th step
Polymer removal
Plasma strip

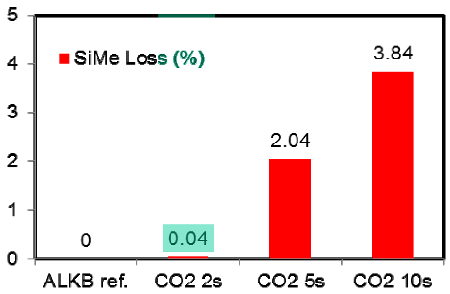
- Cu/Low-k integration flow with polymer pore stuffing (P4 approach, G. Dubois *et al.*)
- Polymers suppress the penetration of reactive radicals → lower C depletion
- Supressed TaNTa penetration
- Material: PECVD p-OSG, k value @ 100kHz is 2.0, open porosity is 46%

Polymer Stuffing

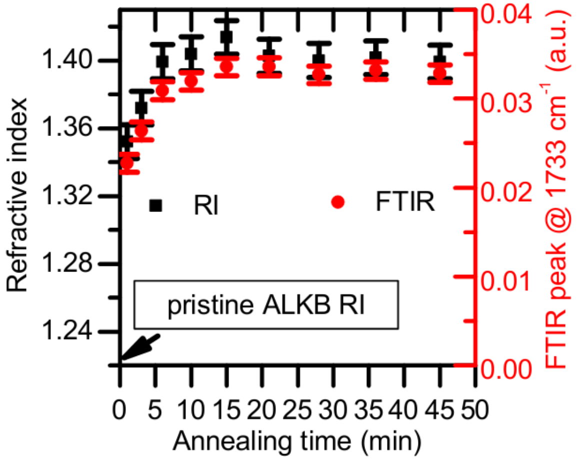


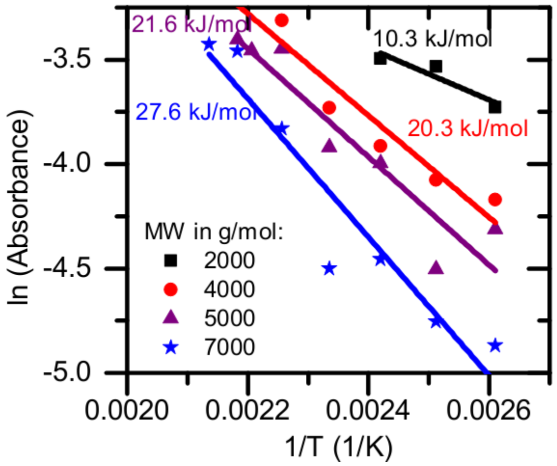






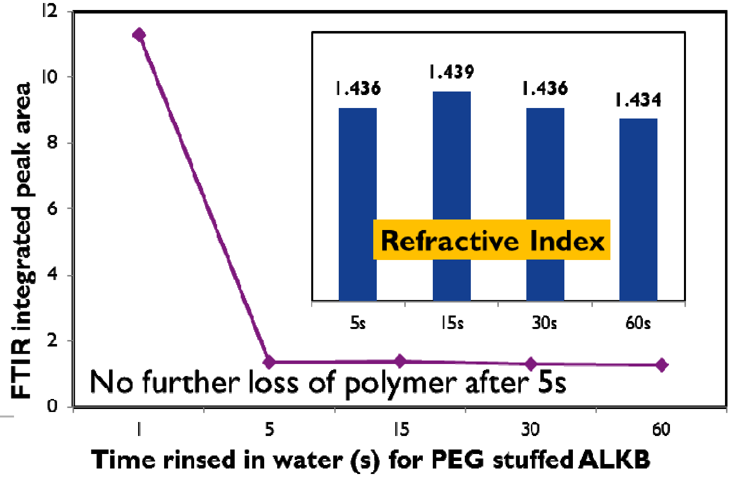
- De-wetting issue due to ultra-low surface energy of low-k. A surface activation process by CO_2 plasma is used.
- Polymer penetration is driven by capillary force, affected by molecular size, pore size and annealing conditions.





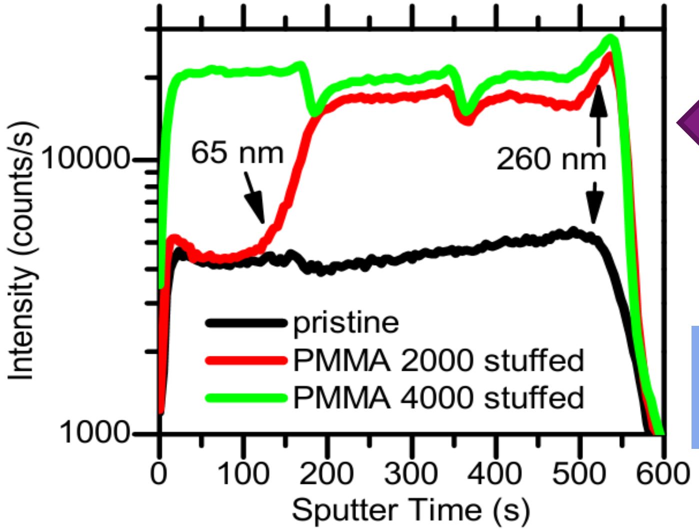
Surface polymer removal

- Solvent need to be adapted to polymer (PGMEA for PMMA, Water for PEG)
- Preferably high surface tension that dos not wet low-k → polymer inside low-k will not be removed.
- Solvent spin cleaning process is optimized to avoid surface polymer depletion.



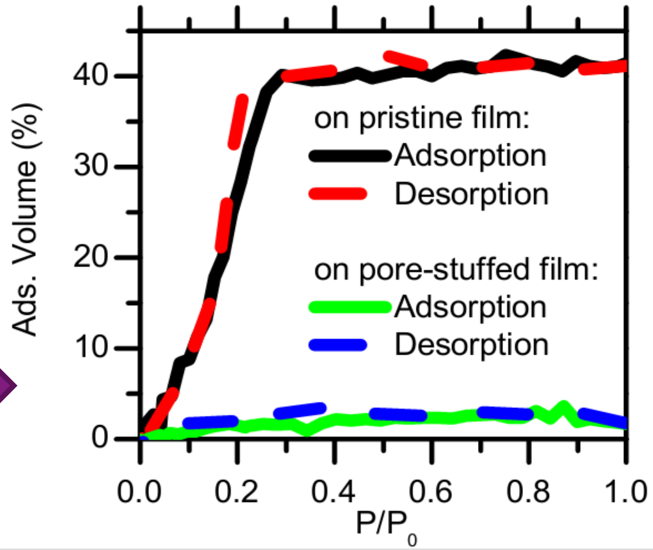
(a) TOF-SIMS carbon depth profile shows polymers penetrate into bulk low-k until bottom. Surface depletion layer is observed for over removal process.

(b) Ellipsometer Porosity with 0% open porosity, confirming the stuffed state.

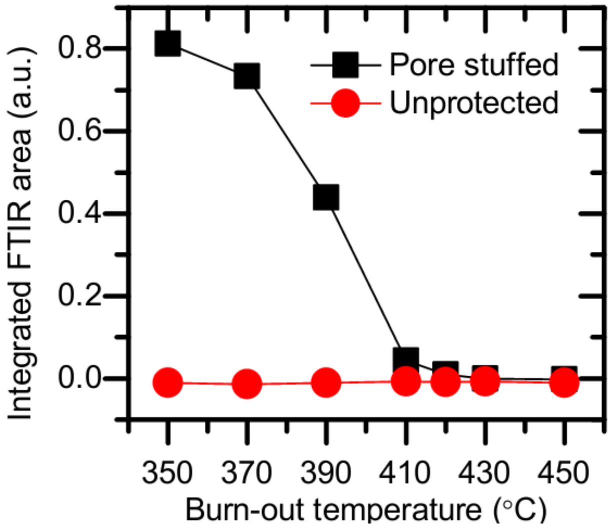


TOF-SIMS Carbon depth profile

Ellipsometry Porosimetry



Polymer unstuffing

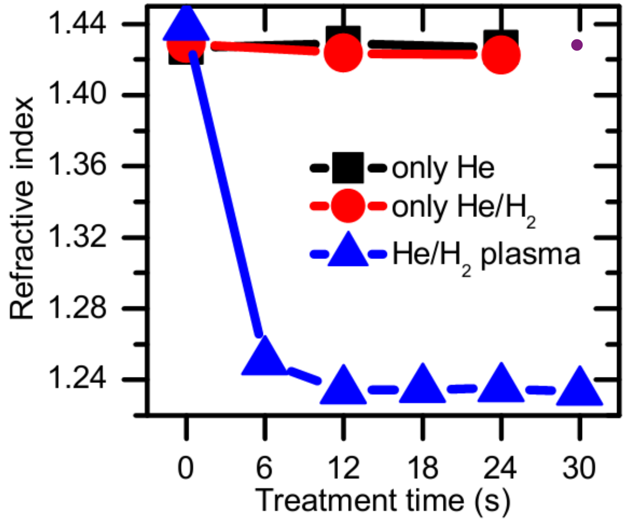


Polymer removal by thermal annealing

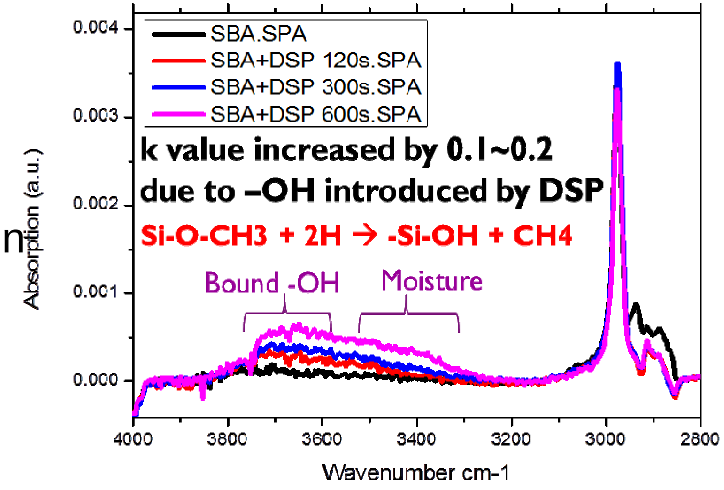
- Polymer degradation process → no low-k damage
- Limited by BEOL process thermal budget (< 420°C)

	AZa	PMMA	AZb	PEG	PS
Thermal Stable Temperature	240	250	293	320	370
Thermal unstuff Temperature	431	400	487	507	499

Polymer removal by downstream plasma (DSP)



Low temperature process (250°C), High polymer removal efficiency. DSP causes low-k damage: formation of Si-OH & k-value increase.



k value increased by 0.1~0.2 due to –OH introduced by DSP

Si-O-CH3 + 2H → -Si-OH + CH4

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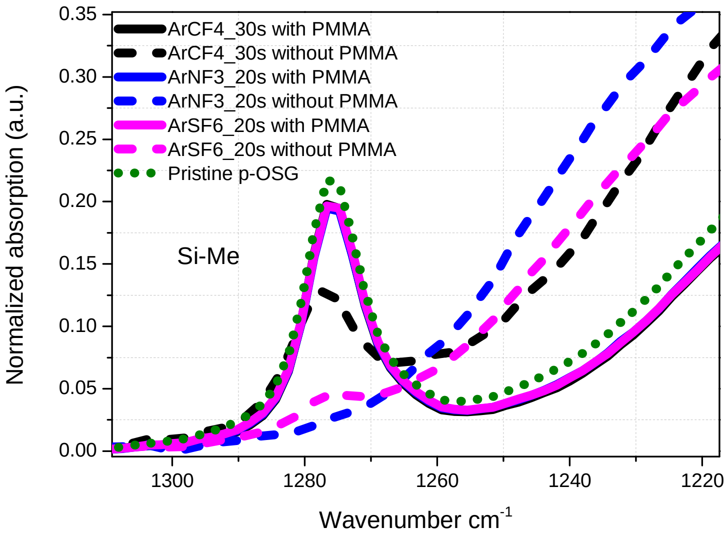
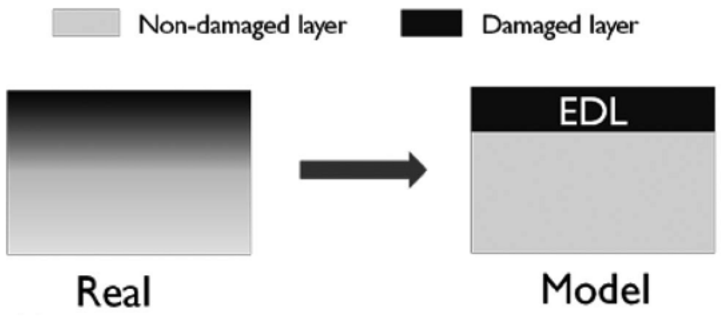
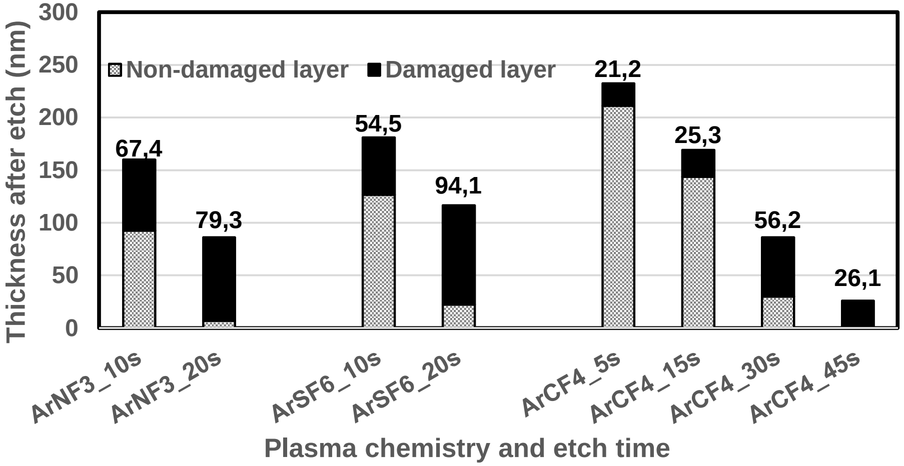
Plasma Induced Damage

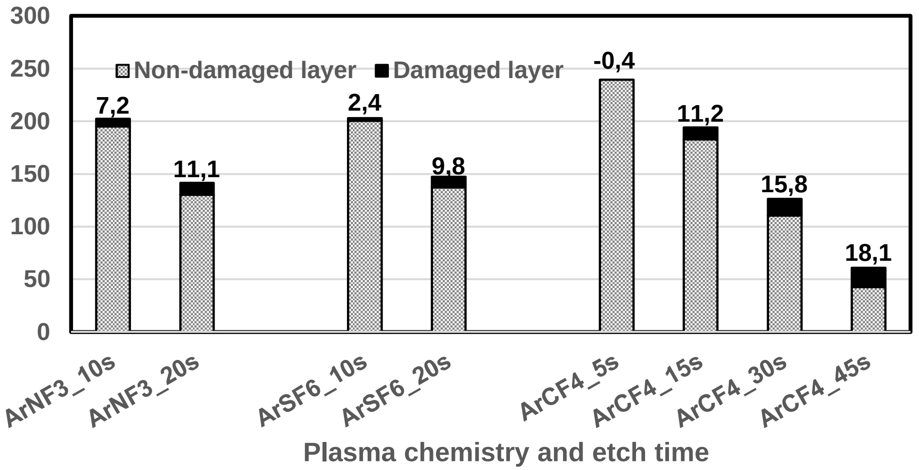




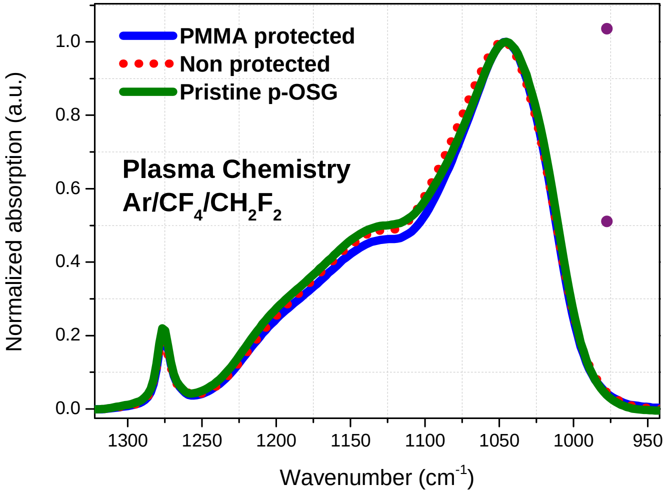
$$EDL = L_{total} - \frac{A_{total}}{K \cdot C}$$

- FTIR enable tracing water uptake and Si-CH_3 loss (PID).
- Based on loss of Si-Me and thickness, Equivalent Damaged Layer (EDL) is calculated.



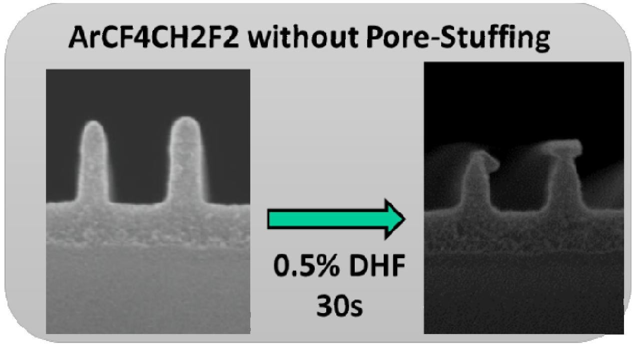


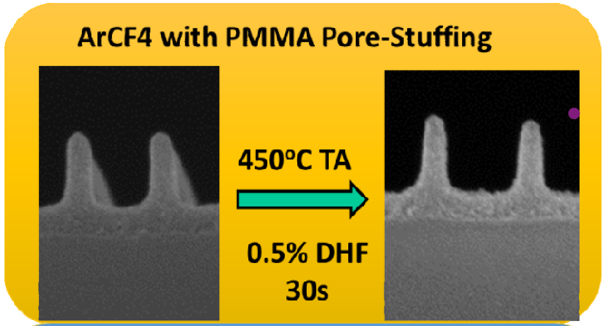
Fluorocarbon gas discharges

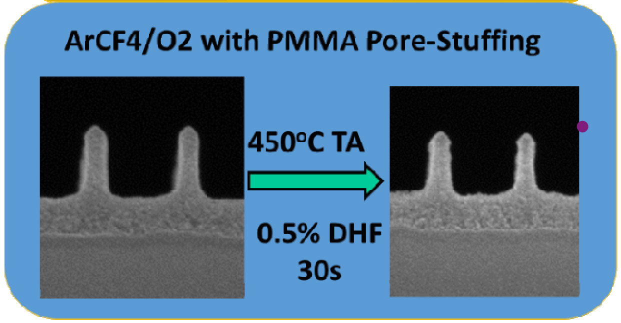


Fluorocarbon plasma is normally used for low-k etching. Due to protection of surface polymerizing effect, low damage is also obtained with blanket test.

However, this does not apply to patterned test, where high sidewall damage is observed.

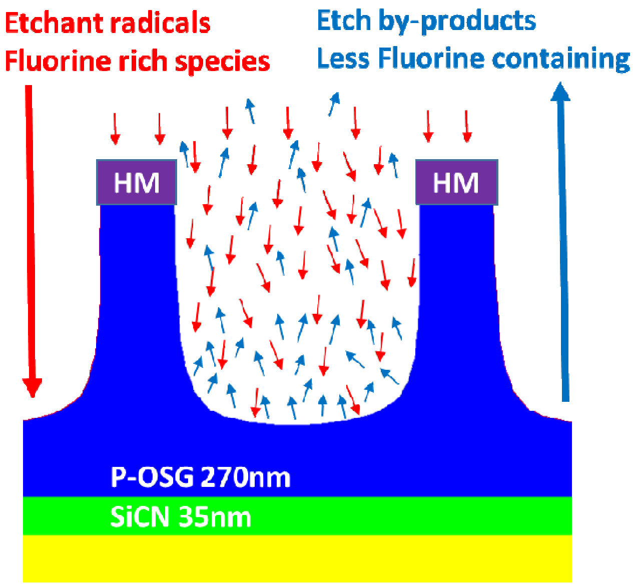

ArCF4CH2F2 without Pore-Stuffing


ArCF4 with PMMA Pore-Stuffing

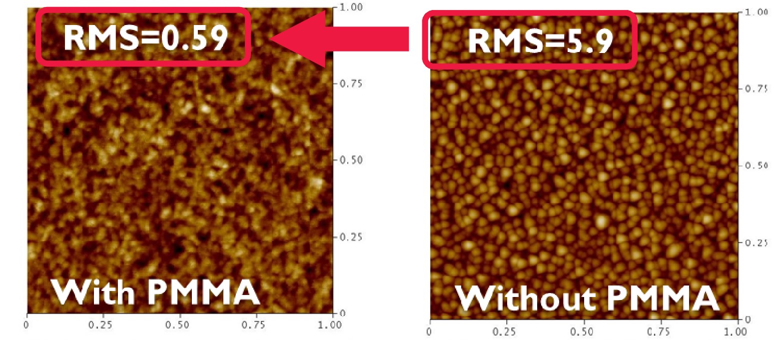

ArCF4/O2 with PMMA Pore-Stuffing

With Pore stuffing, sidewall damage is greatly improved even with O2 containing plasma.

Trench etch condition is quite different from blanket film etching.

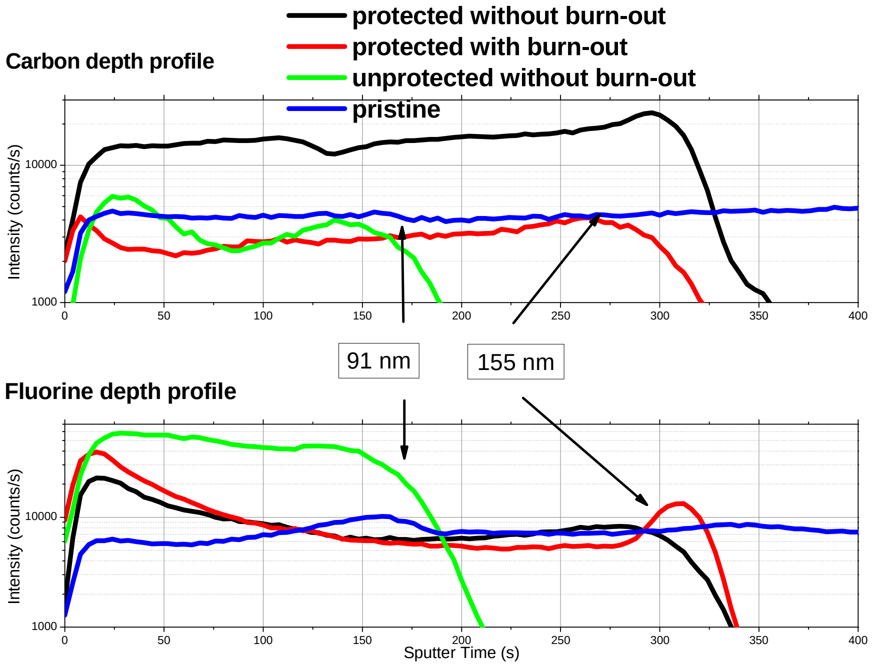


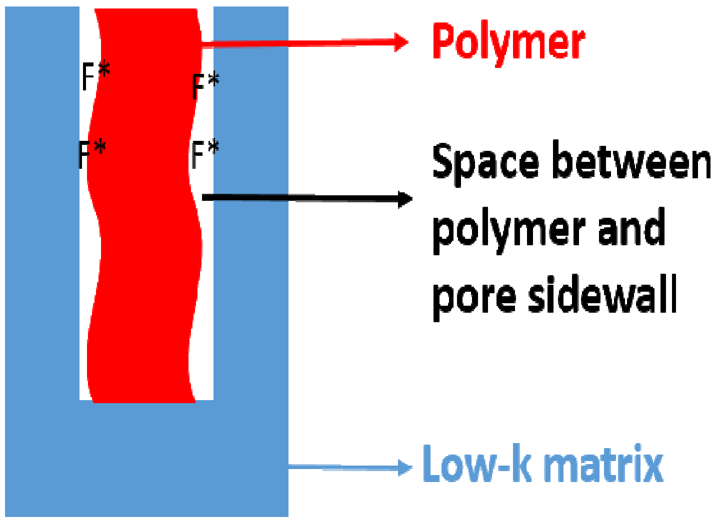
Protection Mechanism



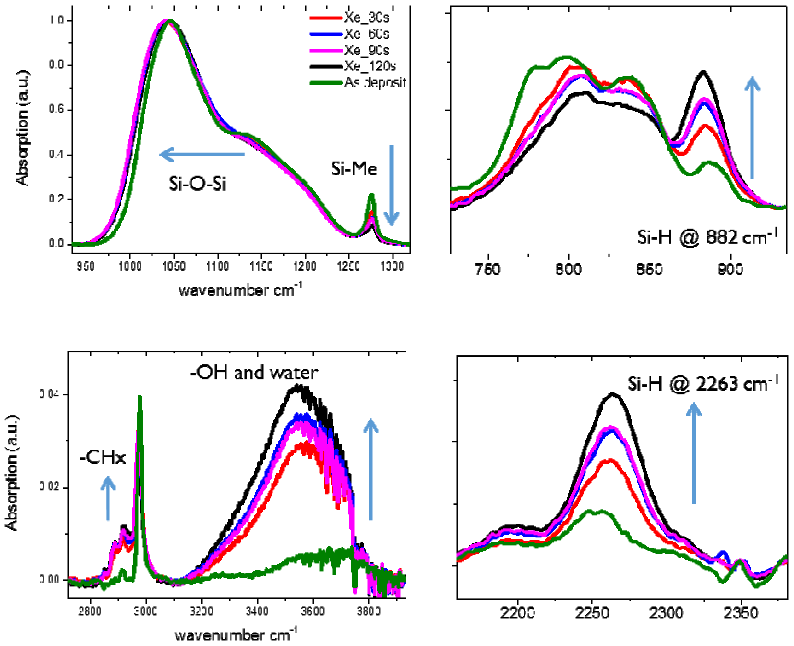
AFM surface roughness for ALKB after ArCF4 etching

- Surface roughness is improved, indicating no internal etching (ten times lower than without protection).
- TOF-SIMS shows reduced F penetration after etch for pore stuffing, compared to porous low-k.





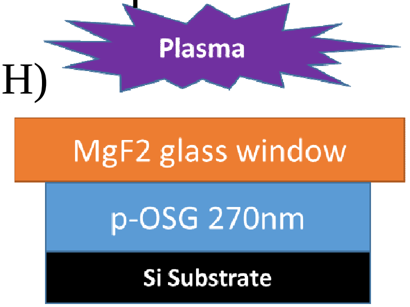
VUV induced damage



- 147nm Xe VUV light (CCP) was used for VUV damaging test, using a MgF_2 glass window.
- FTIR results show loss of Si-CH_3, increasing of Si-H and water uptake.

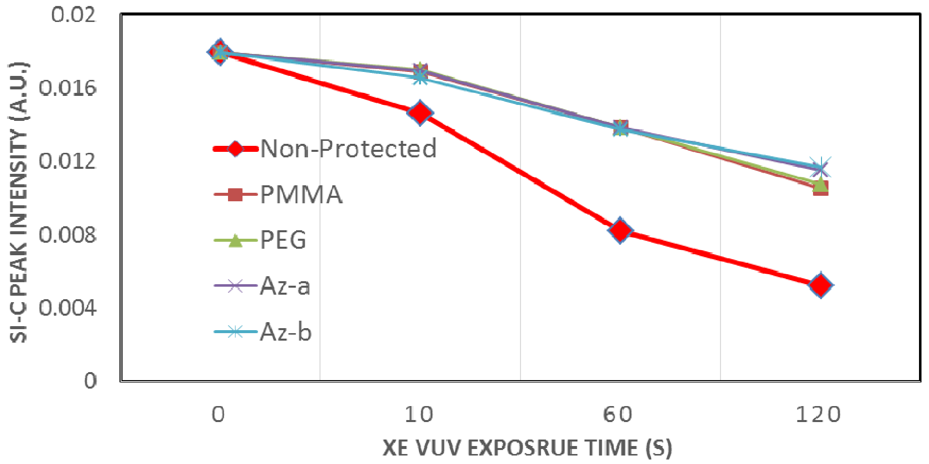
$$O_3\text{-SiCH}_3 + eV \rightarrow O_3\text{-Si}\cdot + CH_2(H)$$

$$O_3\text{-SiCH}_3 + eV \rightarrow O_3\text{-SiH}$$



- Polymers with various VUV absorption were stuffed to check their VUV protection against Xe light.

- Slightly different Si-CH_3 loss is observed with stuffing materials.



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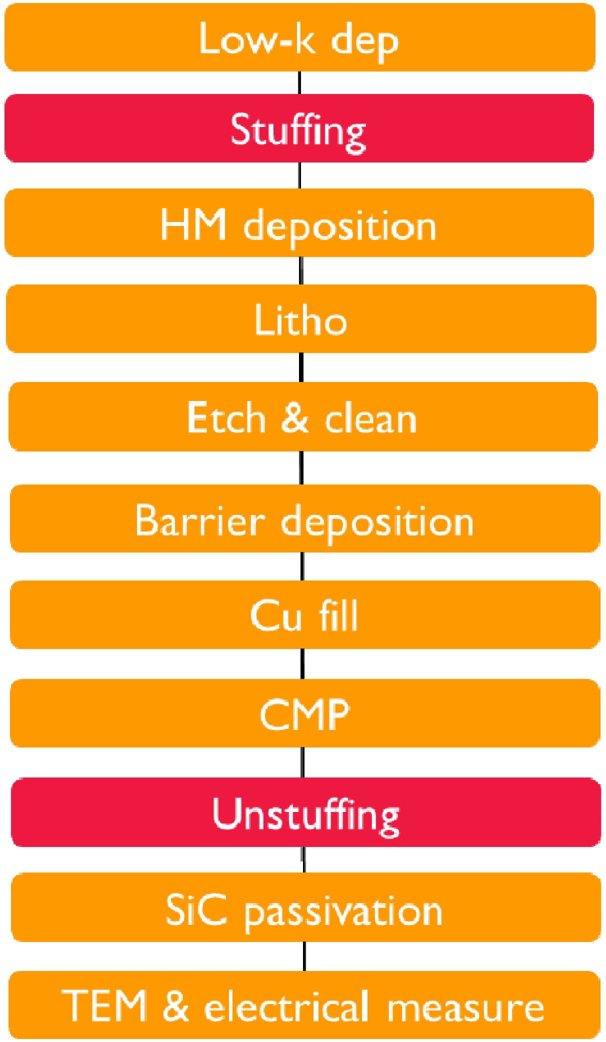
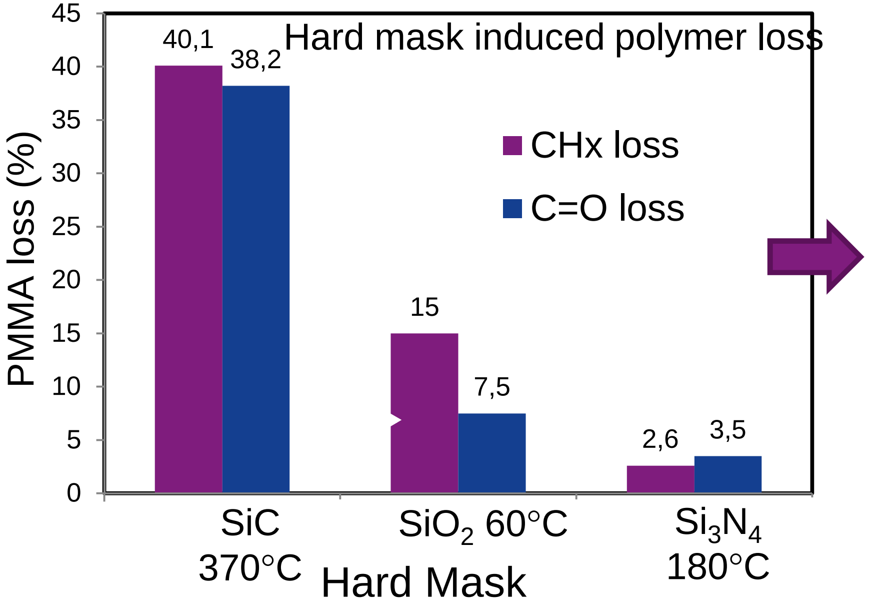
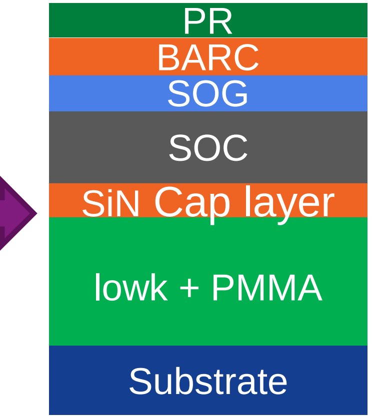
300mm integration flow using PMMA



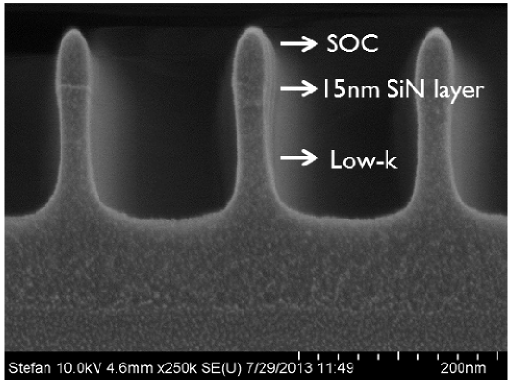




Hard Mask stack

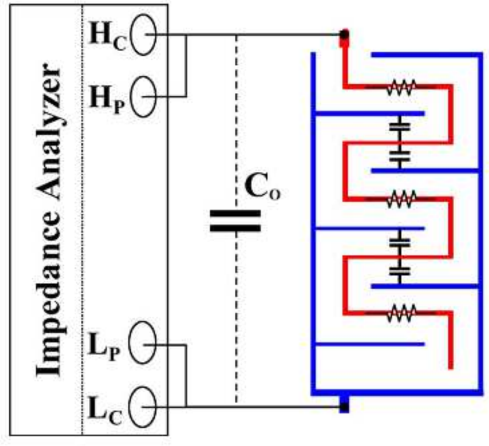
Temperature should be < 200°C and no oxidizing gas

- Narrow spacing hanging trench structure is formed in order to evaluate inter-Cu line effective k-value.
- Polymer is removed after metallization and CMP.

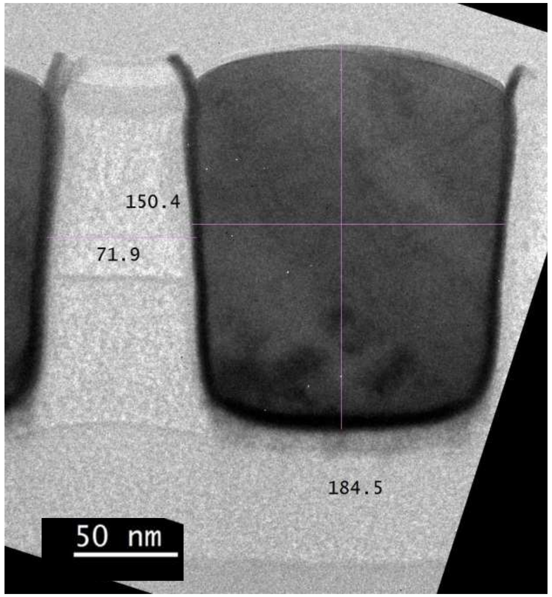


Cross section after HM open and low-k etch

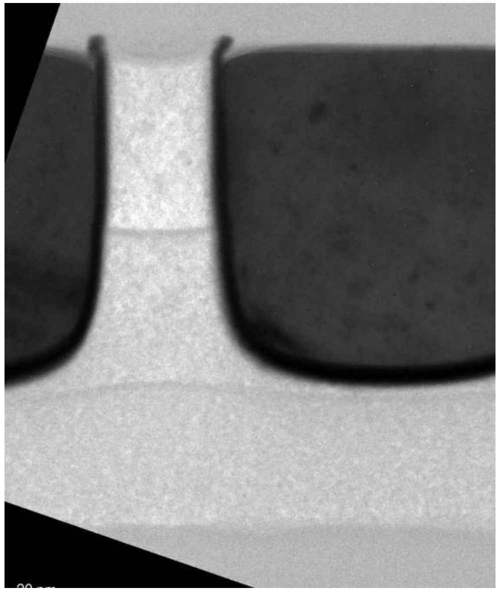
Integrated k-value



No stuffing
Sylilation



PMMA stuffing
Post-CMP unstuffing



K values : **2.89 ± 0.24** **2.64 +/- 0.20**

- TEM pictures are taken to simulate integrated k value.
- Pore stuffing enable lower integrated k value.
- In the case of post CMP unstuffing, the sharp interface between barrier and low-k reveals no penetration of barrier.
- Residual damage is tentatively attributed to PMMA removal process

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Summary

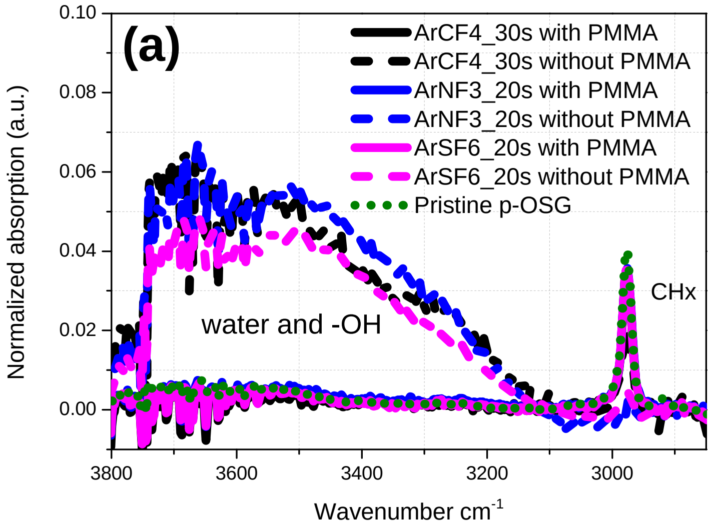
- Following by surface active, spin-coating, thermal drive-in and surface cleaning, > 90% pore-stuffing of a 2.0 porous OSG was achieved.

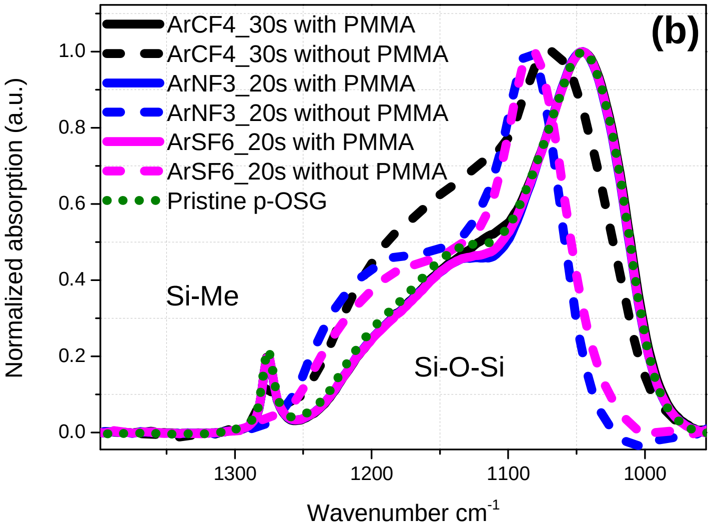
- Reduced plasma induced damage is observed, based on various plasma tested on both blanket and patterned samples. VUV induced damage is also improved.

- Single damascene Cu/Low-k integration flow on 300mm substrate has been developed incorporating pore stuffing approach.

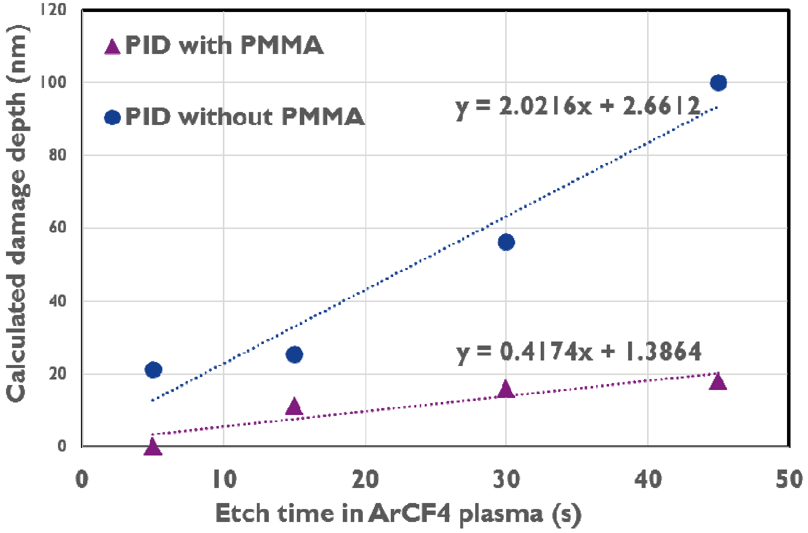
ASPIRE
INVENT
ACHIEVE

Plasma induced damage

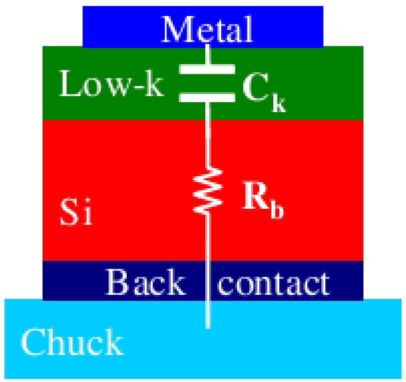




Plasma induced Damage



- PID increases with etching time or etching depth.
- With Pore-Stuffing, PID penetration rate is improved by 80%.
- With formation of front and back electrodes, Ck is measured and k value could be extracted. With Pore stuffing, k value can be well controlled during plasma process.



k-value at 100KHz