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TIN/TAN SELECTIVE ETCH IN N10 RMG WITH CHLORINE BASED PLASMAS

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OUTLINE

N10 CMOS RMG process flow

- pMOS 1st stop on high K
- pMOS 1st stop on TaN

TiN /TaN selective etch for pMOS 1st stop on TaN approach

- TiN/TaN selective etch mechanism
- Native oxide layer break through study
- TiN and TaN ME study
- TiN to TaN selective etch on N10 RMG device wafer

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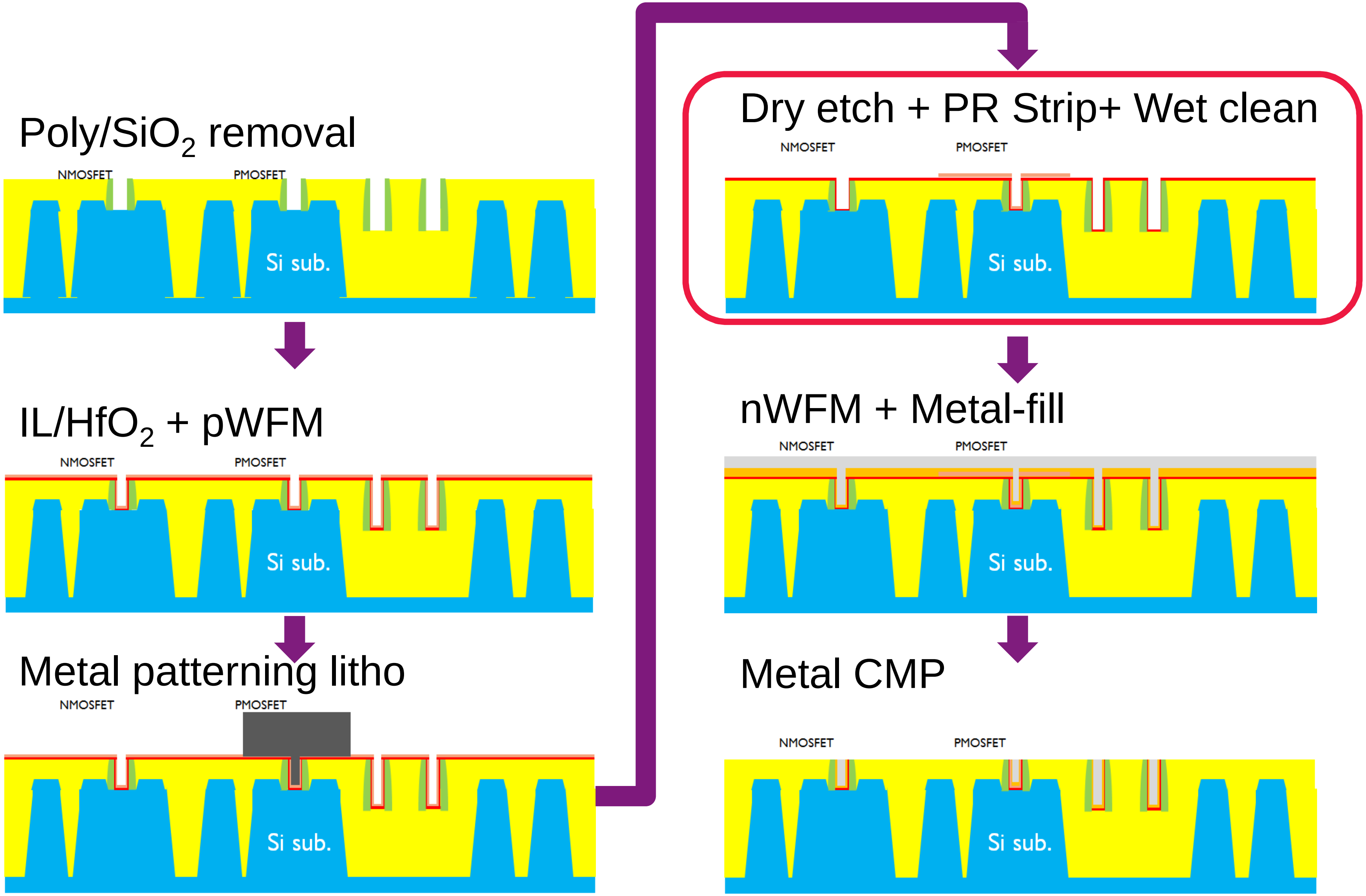
PMOS 1ST RMG PROCESS FLOW



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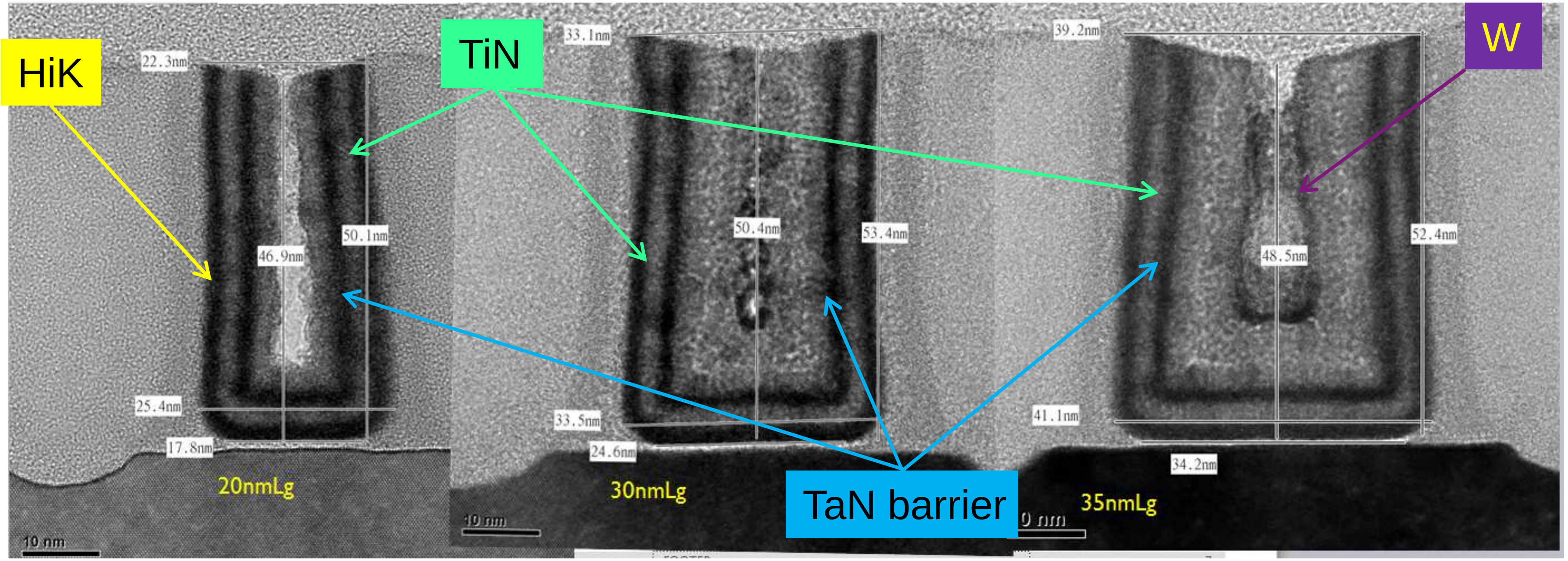
METAL GAPFILL

The major challenge in the RMG module is the gapfill. Current PMOS first CMOS scheme gives limited space left for W Fill. Not straight gate profile also prevent proper filling.



Not even have space for Nmetal stack filling

Gate stack is fully filled by P and N metal stacks, no space left for W.

W is able to fill on top of the P and N-metal stacks

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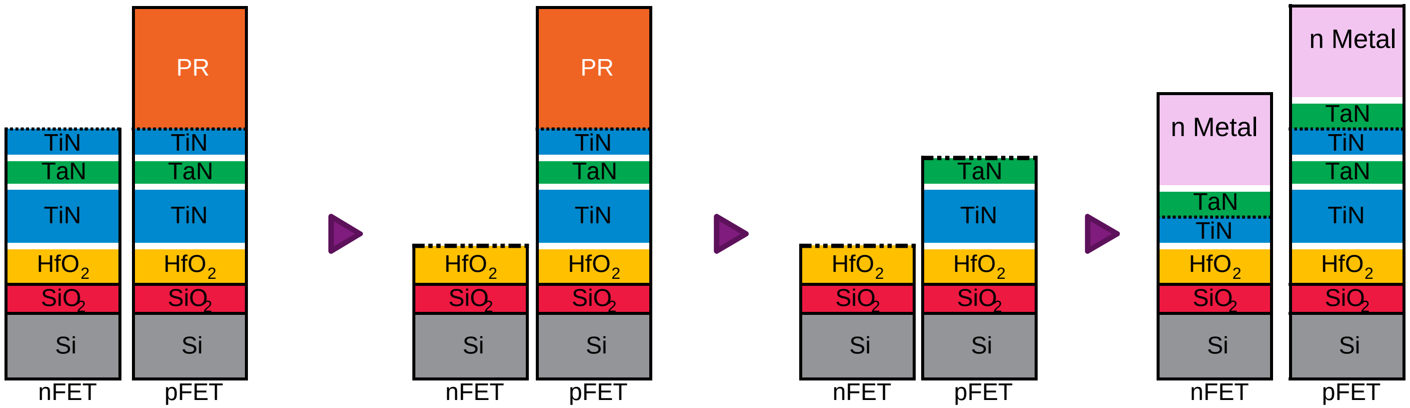
PMOS 1ST STOP ON HIGH K AND STOP ON TAN COMPAREMENT

Stop on high K



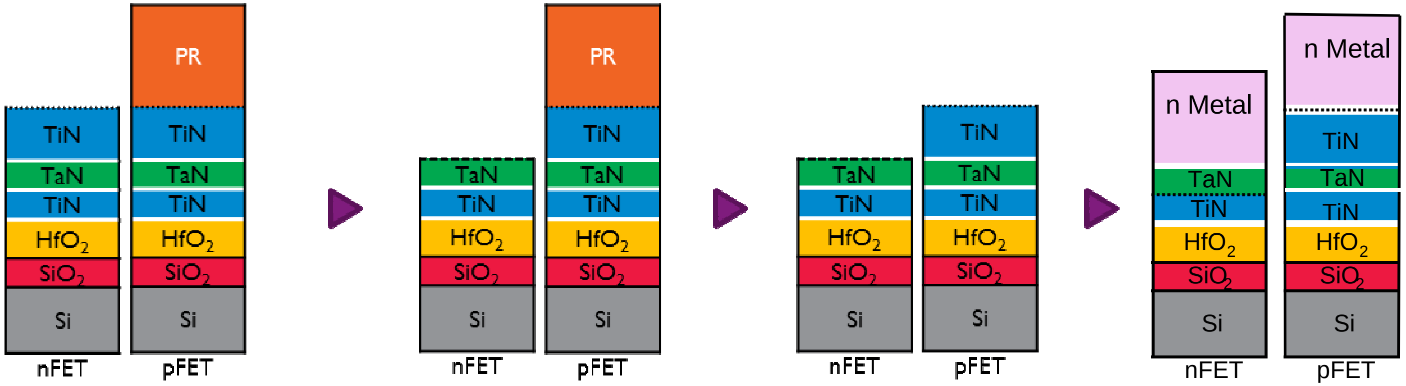
pMetal+ TaN barrier and sacrificial TiN dep + litho

Dry removal of metals from nFET

PR strip +Wet clean

nMetal barrier + Metal filling

Stop on TaN



TiN/TaN/TiN dep + litho

$Cl_2/He/O_2$ etch of TiN from nFET

PR strip + wet Clean

nMetal filling

Selective etch between two similar metal layers is very challenging.

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TIN TO TAN SELECTIVE ETCH MECHANISM

- TiN to TaN selective etch may be achieved with a low temperature Cl_2 based process, because the volatility of TiCl4 is higher than TaCl5.

TiN+Cl2 → TiCl4 (BP136.4C)+N2 (easy),
TaN+Cl2 → TaCl5 (BP239.4C)+N2(less easy)

- High selectivity of TiN to TaN could be achieved by introducing an oxidize plasma etch chemistry which is favouring etch stop on TaN by TaO formation on the surface.

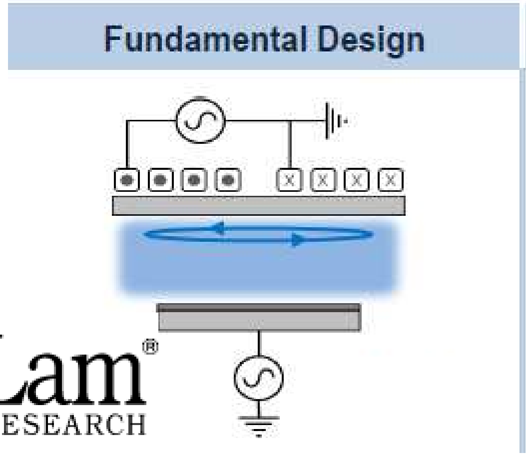
TaCl5+O2 → TaO+Cl2 (easy)
TiCl4+O2 → TiO+Cl2 (less easy)

Bond dissociation energy 298k KJ/Mol
Ta-N 611, Ta-O 805, Ta-Cl 544,
Ti-N 464, Ti-O 662, Ti-Cl 494,

EXPERIMENTAL

- Material etch rates were measured on blanket 10nm thick ALD TiN or TaN layers. Etch experiments were carried out on a 300mm **Lam Research 2300®Kiyo® TCP** plasma etch system.

- For all experiments, a BCl3 based break through (BT) step was added to remove the native oxide layer on the surface, otherwise further etching would be impossible.



Lam® RESEARCH

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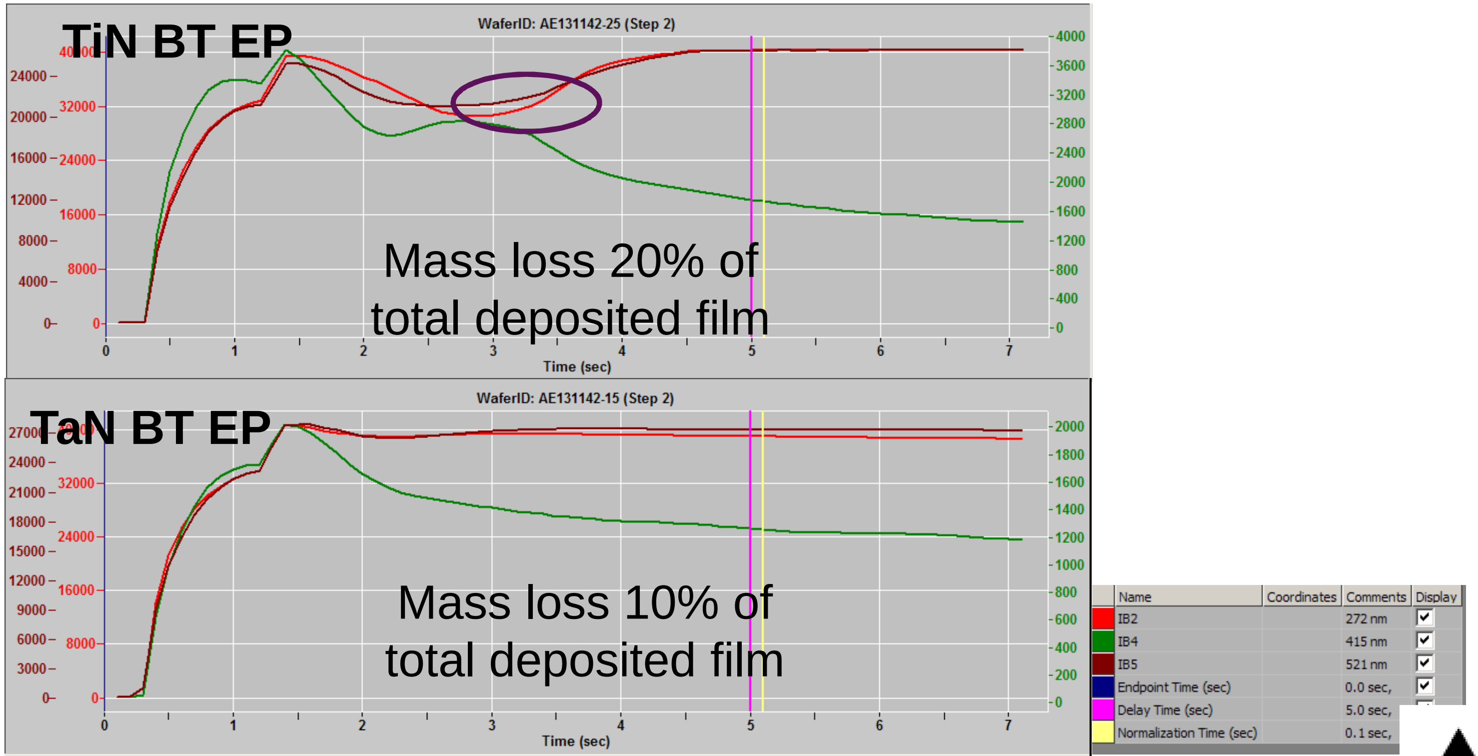
BT STEP STUDY

- BT needed to enable metal etch
- BT step study for TiN and TaN
  - TiN BT: BCl3 base 50v bias power
  - TaN BT: Etching stop was observed with same BT step. Increase to 100v bias BT step to resolve etching stop issue.



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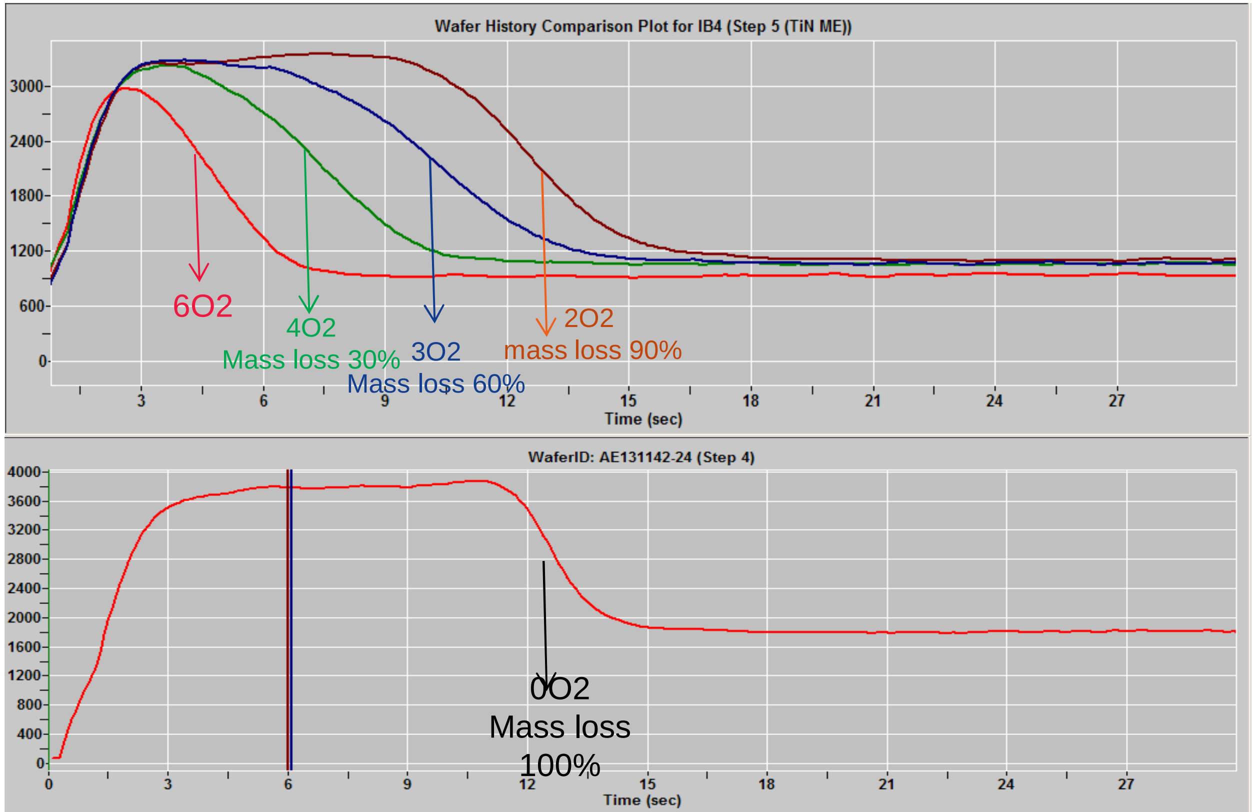
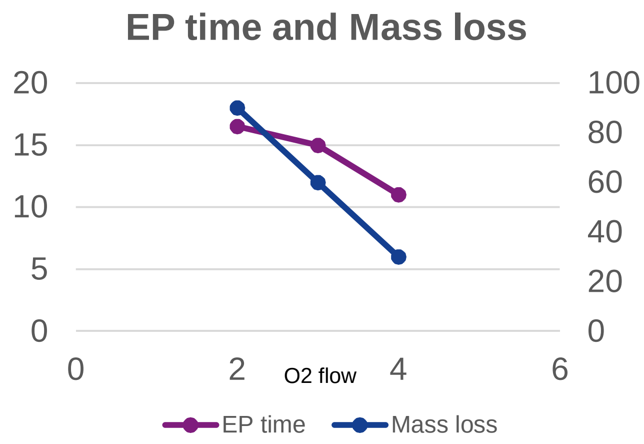
TIN ME STUDY 1

- TiN ME study: Cl2/He base process with O2 addition

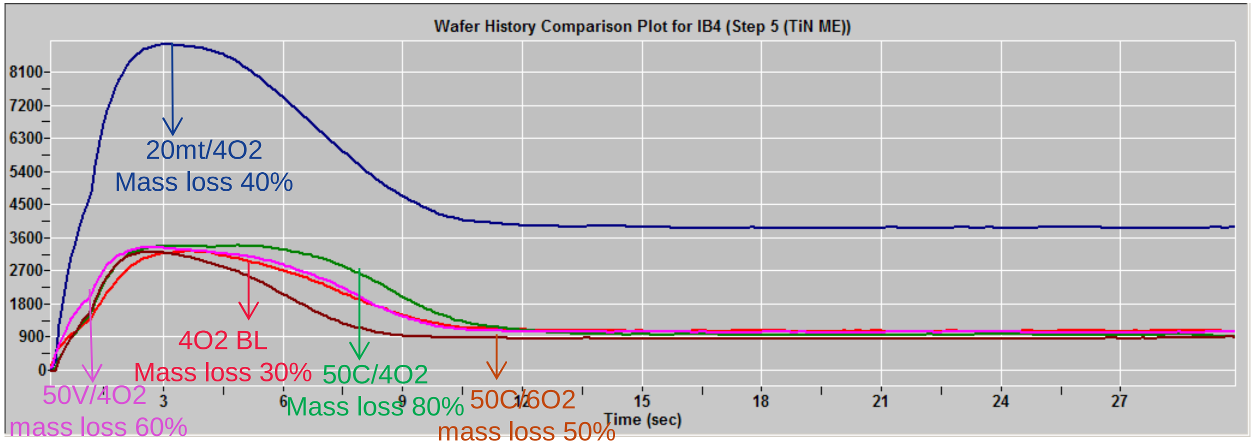




O2 addition causes TiN etch stop due to TiO formation

TIN ME STUDY 2

- TiN etch process trends study: Cl2/He with 4O2 addition
  - BL = high P / zero bias / T < 50° C

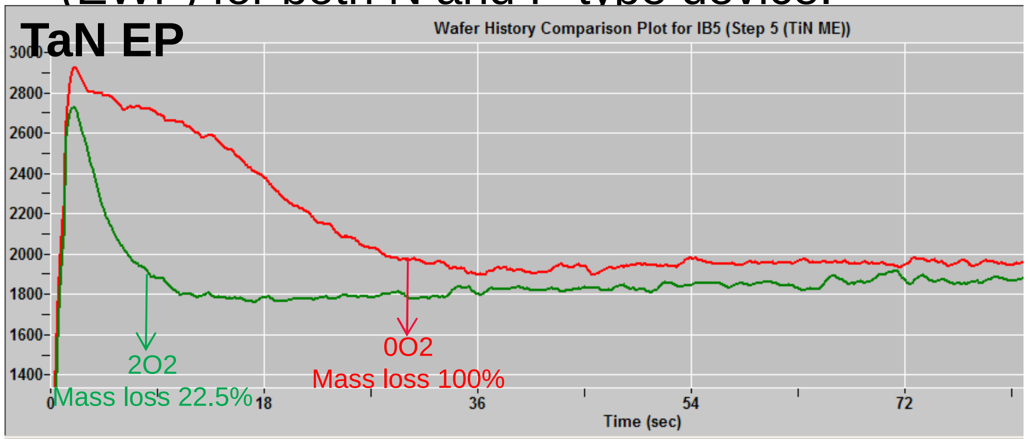


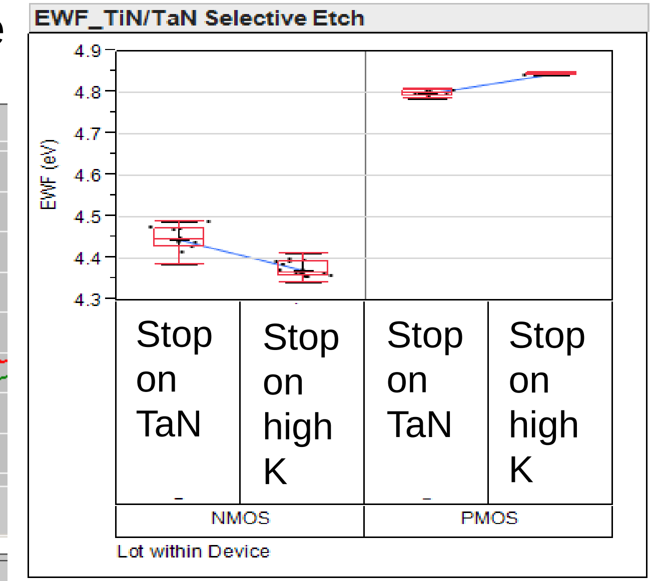
	20mT	50v bias	50°C	BL
EP time	10s	10s	11s	10s
Mass loss	40%	60%	80%	30%

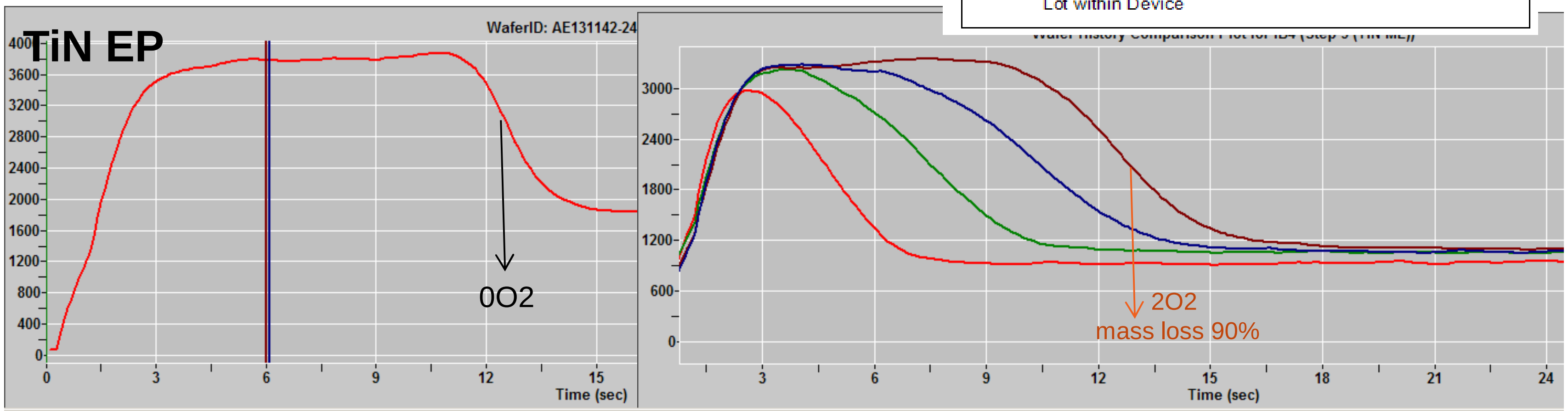
Ti oxidation step not sensitive to P and bias
Sensitive to T and O2 flow: chemically driven

TAN ME STUDY

- TaN ME study: Cl2/He base process with O2 addition
  - ~2:1 TiN-to-TaN selectivity was achieved with Cl2/He only process.
  - Etching stop of TaN was observed by adding 2sccm O2 in Cl2 based process.
  - The best results obtained on blanket wafers have been transferred to planar devices wafers. There is no shift in the (EWF) for both N and P-type device.







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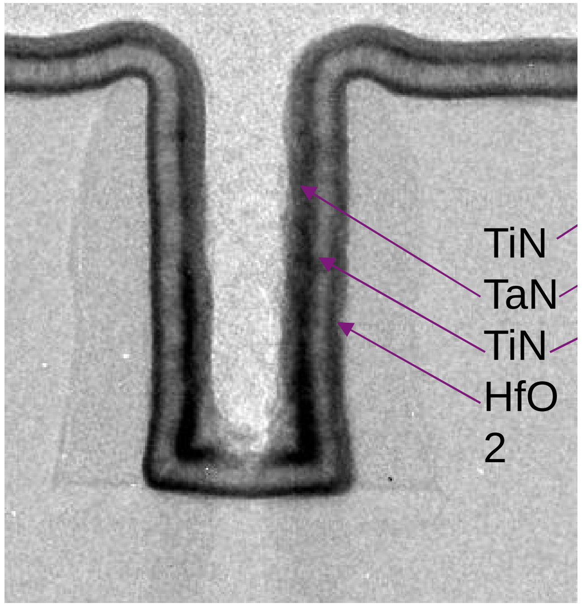
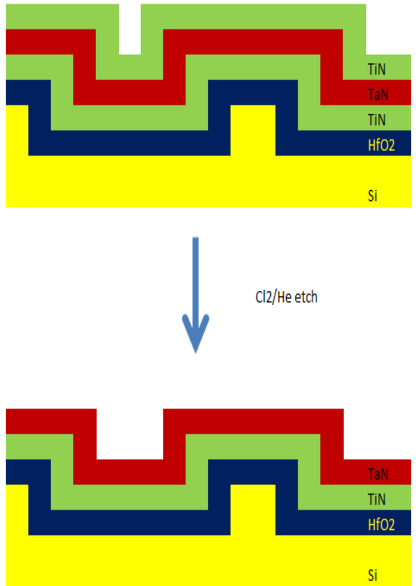
N10 RMG TIN/TAN SELECTIVE ETCH RESULT

- Selective etch 5nmTiN over 3nmTaN: Cl2/He/2O2 base process.
  - TiN was fully removed selectively to the oxidized TaN in 40nm gate structure.
  - Etch stop was observed in the 20nm and 30nm gate structure due to full fill. Thin down the WFM TiN-TaN-TiN trilayer to keep enough gap space is important for the future device scaling.



40nm Gate



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SUMMARY

- pMOS 1st stop on TaN approach can avoid highK layer exposed to plasma and has more space for Metal deposition.
- High TiN to TaN selectivity can be achieved by introducing O_2 into Cl_2/He plasma.
- PMOS 1st stop on TaN and stop on highK approach got comparable device performance on planer device wafer.
- 5nm TiN was fully removed selectively to 3nm TaN in N10 RMG for 40nm gate structure.
- However, an etch stop was observed in the 20nm and 30nm gate structure. Thin down the WFM to keep enough gap space is important for future device scaling.

ACKNOWLODGEMENTS

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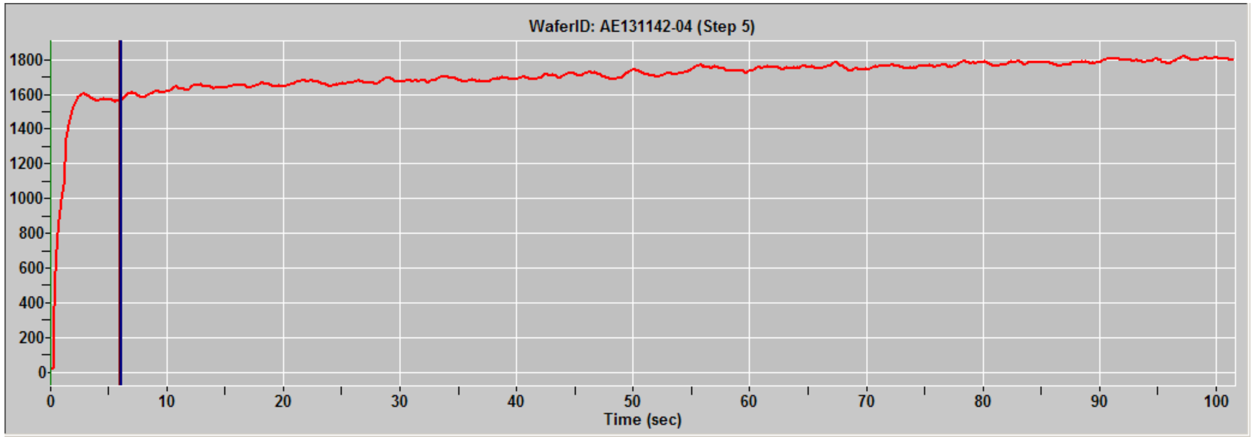
- Specially thanks to MCA team, Jef Geypen, Paola Favia and Hugo Bender for TEM support.

ASPIRE
INVENT
ACHIEVE

TIN AND TAN ETCH WITHOUT BT STEP

- Etching stop was observed without BT step: ME only Cl2/He base
  - TiN EP **OES 415nm**, no obvious EP and mass loss observed.



  - TaN EP **OES 521nm**, no obvious EP and mass loss observed.