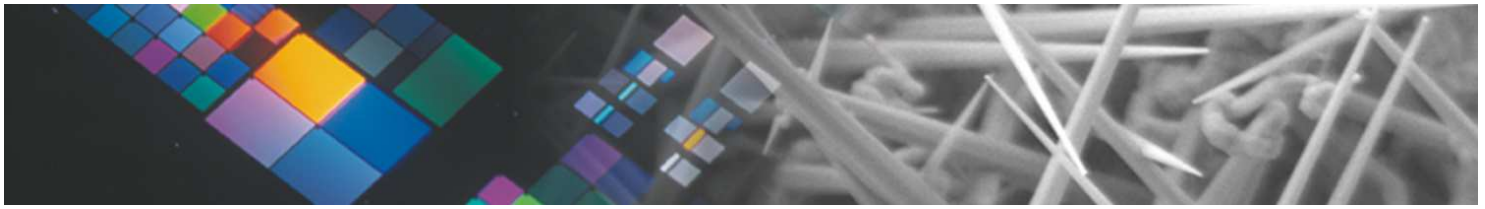

Sidewall roughness characterization of a 20 nm half pitch resist-core spacer patterning process

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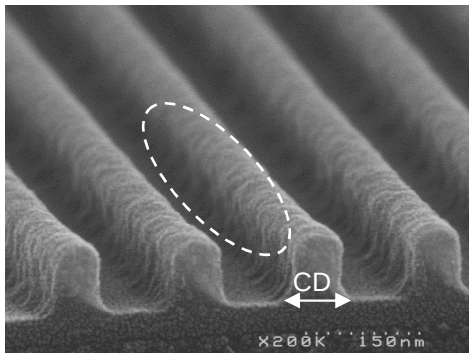
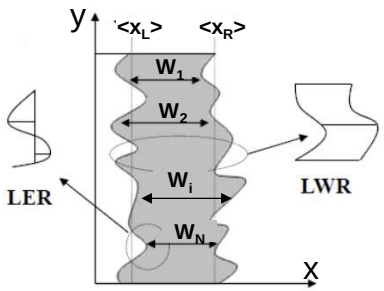
PESM 2014 Conference
2014.05.13 - Grenoble, France

Outline

- Introduction
- Development of a spacer patterning process for the 20 nm node
- Characterization of the sidewall roughness

Sidewall Roughness issues



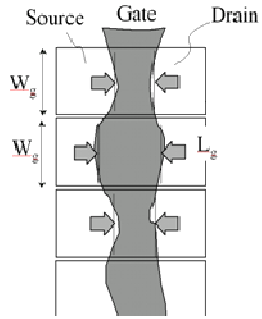


- Line Width Roughness

$$LWR = 3\sigma_{CD} = 3\sqrt{\frac{1}{N}\sum_{i=1}^{N}(W_i - \langle W \rangle_N)^2}$$

- Line Edge Roughness

$$LER_{Left} = 3\sigma_L = 3\sqrt{\frac{1}{N}\sum_{i=1}^{N}(x_{L,i} - \langle x_L \rangle_N)^2}$$



- Degradation of transistor electrical performances
  Source of device variability and yield

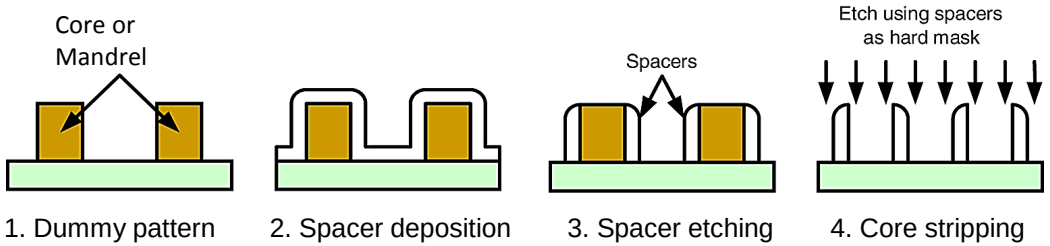
- ITRS specifications : LWR ~ 10% of CD_{target}

- For Sub-20nm nodes, LWR and LER < 2 nm
  - Critical process parameter => **Roughness reduction issue**
  - Resolution limit of measurement instruments => **Metrology tool issue**

➔Need of an accurate and insightful characterization of the sidewall roughness

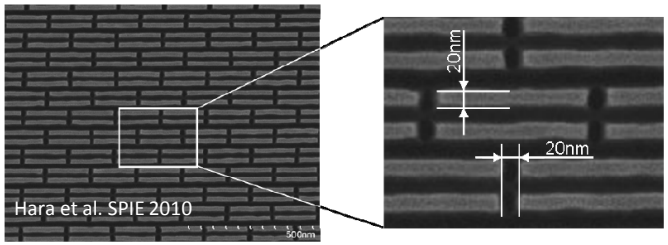
Self-Aligned Double Patterning : SADP

- A Nanopatterning lithography technique

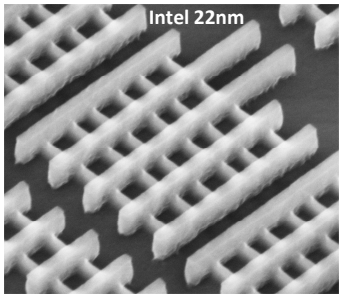


- Dense array of Lines\Spaces structures by pitch division
- Extension of the 193 nm optical lithography resolution limit
- HVM for memory and logic applications

SRAM gate

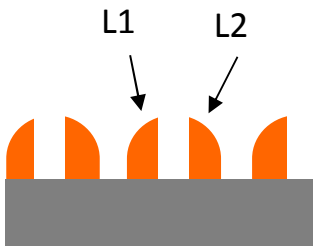


FinFET



- Candidate to the 10 nm node and beyond !

Problematic / Objectives



- Spacers are asymmetric by nature
- 2 populations of lines : L1 and L2
- When they are used as an etch mask, it can result in asymmetric profiles or LER

❑ **Evaluate the LWR and LER** of dense array of lines/spaces structures obtained with a **spacer patterning process** targeting **a 20 nm half-pitch**

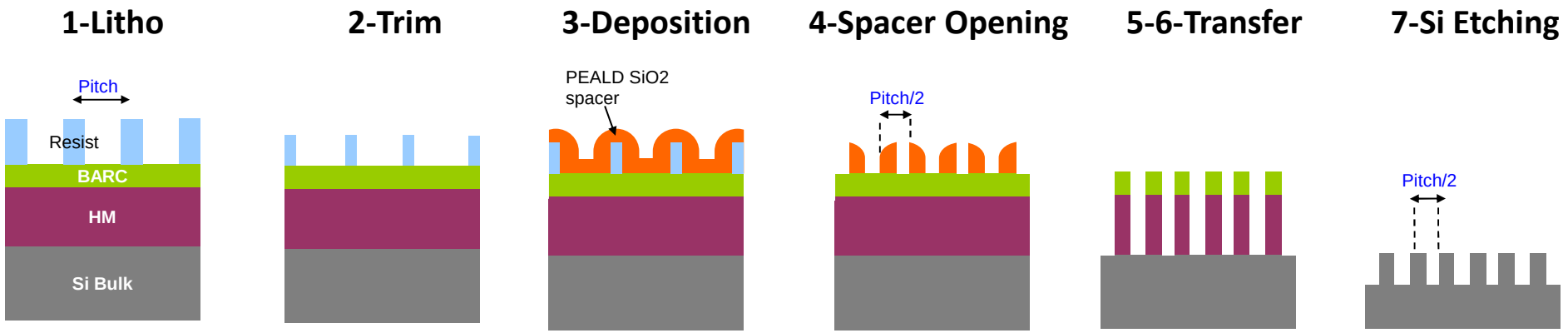
❑ **P**ower **S**pectral **D**ensity method

➔ Unbiased LWR and LER measurements
➔ Spatial frequency analysis of the roughness

Outline

- Introduction
- Development of a spacer patterning process for the 20 nm node
- Characterization of the sidewall roughness

Resist-core spacer patterning process flow



Spacer material is directly deposited on the resist lines

Challenge

- PR are thermally degradable
- CDV Spacers are not compatible

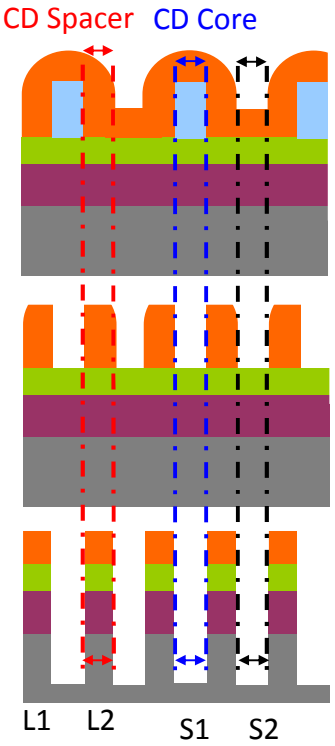
Solution : PEALD

- Low-temperature deposition technique
- Highly Conformal and uniform film
- No loading effect

Benefits of this integration

- Simplified stack
- Less steps than HM approach
- Improved cost of ownership

Key parameters of the SADP process



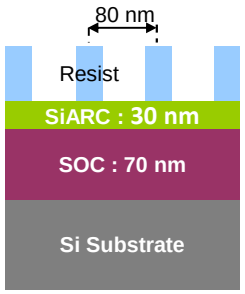
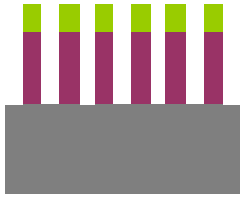
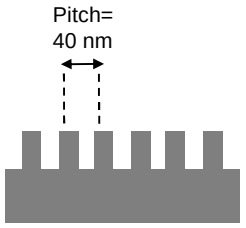
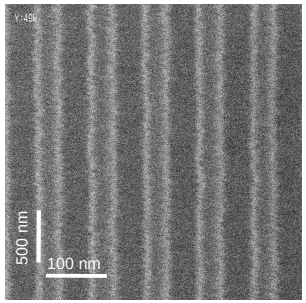
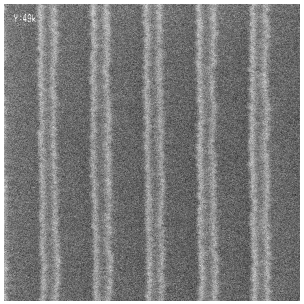
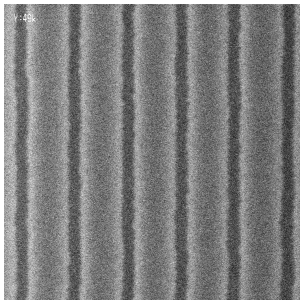
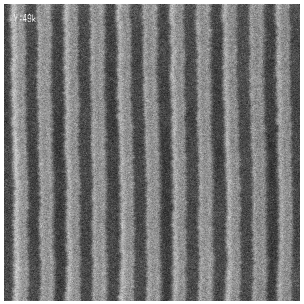
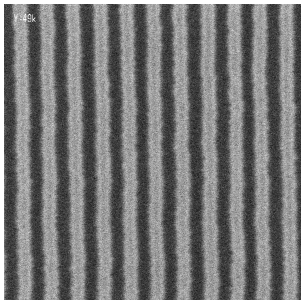
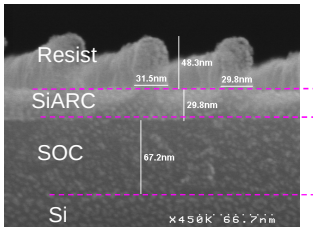
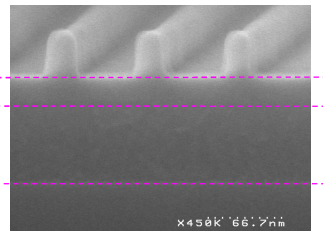
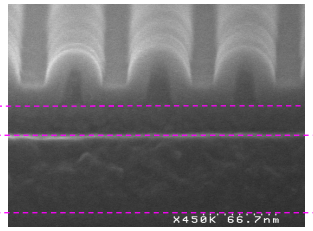
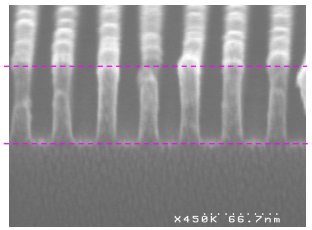
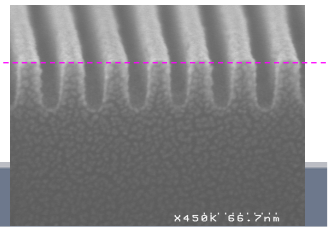
To control the width of the final lines and spaces, one can play with two parameters :

- CD Spacer ➔ CD L1 and L2
- CD Core ➔ Space S1

} ➔ Space S2

LTM
LABORATOIRE DES TECHNOLOGIES DE LA MICROÉLECTRONIQUE

20nm HP Optimized Process

	1-Litho	2-Trim	3-Deposition	4-Spacer Opening	5-6-Transfer	7-Si Etching
						
Process infos	E-beam resist lines	Resist : HBr / O_2 CD_{trim} =CD_{theo} +10nm	SiO_2 spacer by PEALD 20nm @ 50°C	Spacer : CF_4 Resist Stripping : O_2	SiARC : CF_4 / CHF_3 / Ar SOC : HBr / 02	Si: SF_6 / CHF_3 / Ar Spacer stripping : O_2
CDSEM						L=S=20nm CDU (3σ) < 2 nm
XSEM						

Outline

- Introduction
- Development of 20 nm HP spacer patterning process
- Characterization of the sidewall roughness

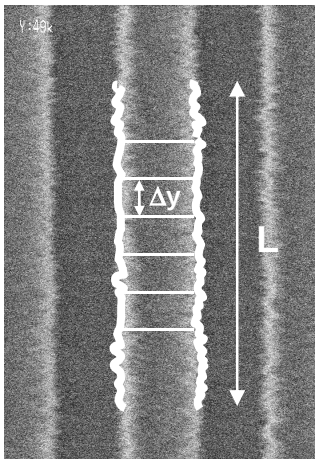
Sidewall roughness Characterization

- Unbiased LWR and LER measurements from CD-SEM images

$$\sigma^2_{meas} = \sigma^2_{real} + \sigma^2_{noise}$$

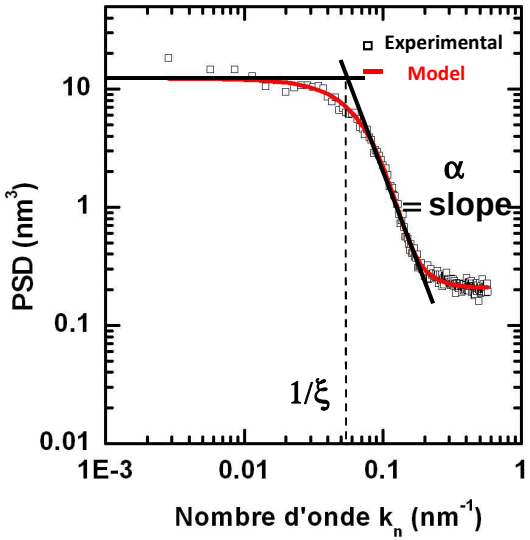
- **P**ower **S**pectral **D**ensity method ➔ Spatial frequency analysis of the roughness

CD-SEM line segments (N*)



N*>200
L=2154nm; Δy=5.4nm

Average PSD calculation



Fit the PSD with FFT of ACF

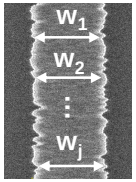
ACF : $R(u) = \sigma^2 e^{-|u/\xi|^{2\alpha}}$

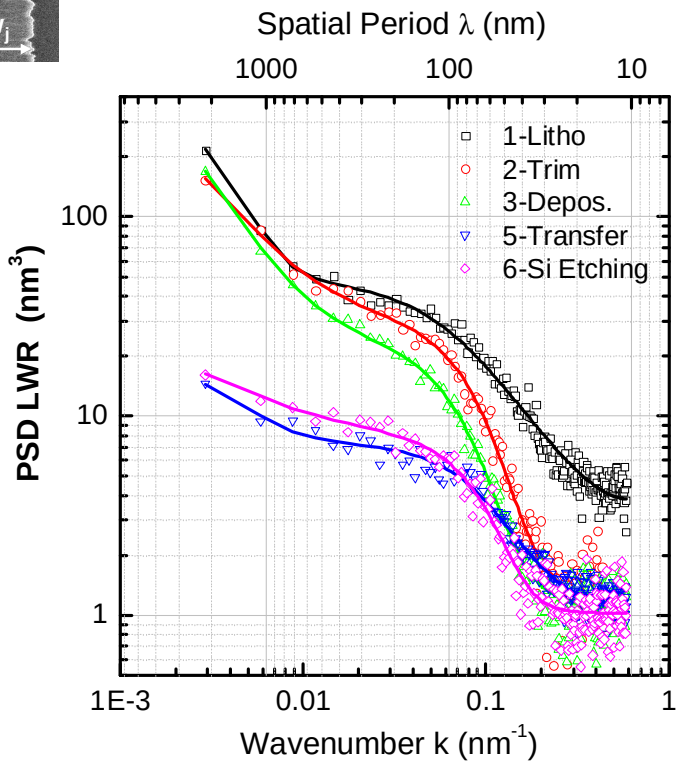
$$P_n = \frac{\Delta y}{2\pi N}\sigma^2_{réel}\left[\sum_{m=0}^{N-1} 2k^{-\left|\frac{m\Delta y}{\xi}\right|^{2\alpha}} \cos\left(k_n m\Delta y\right)(N-m)\right] + \frac{\Delta y}{2\pi}\sigma^2_{bruit}$$

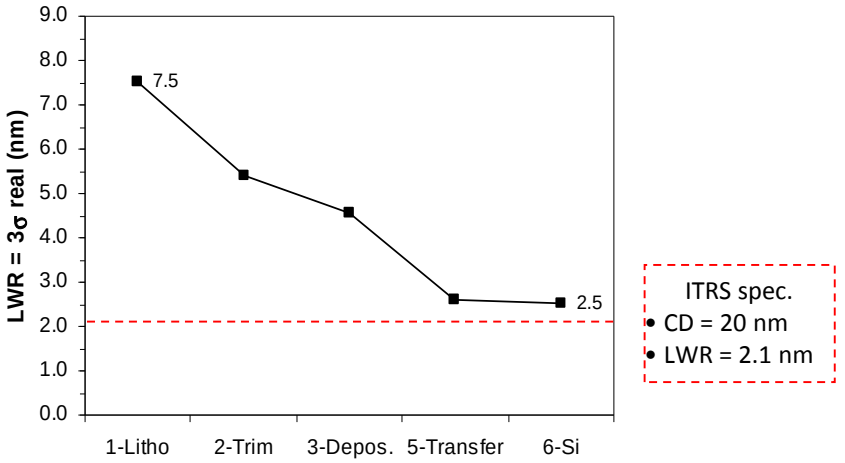
L. Azarnouche et al. JAP 2012

Extraction of
- σ_{real} : amplitude
- ξ : correlation length
- α : fractal exponent

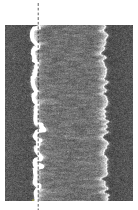
LWR

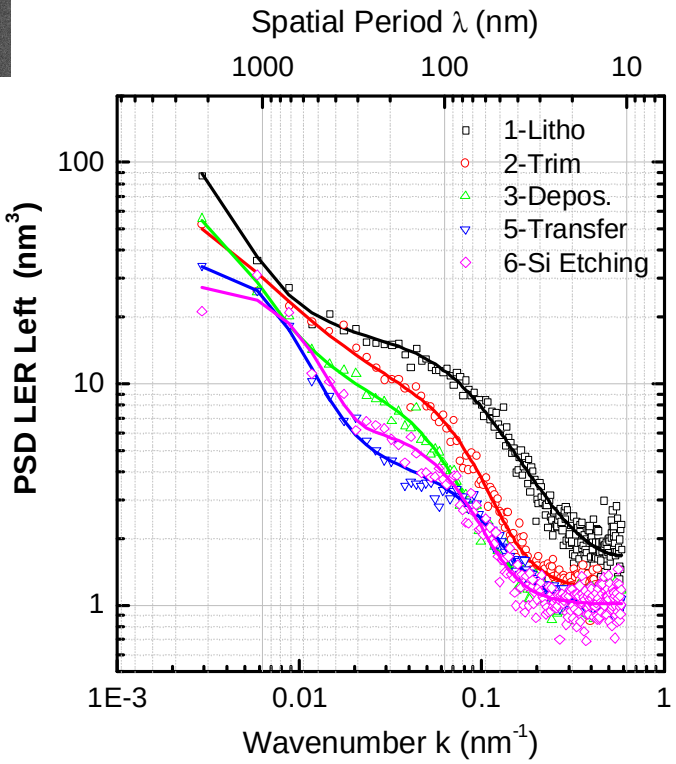

W1
W2
Wj

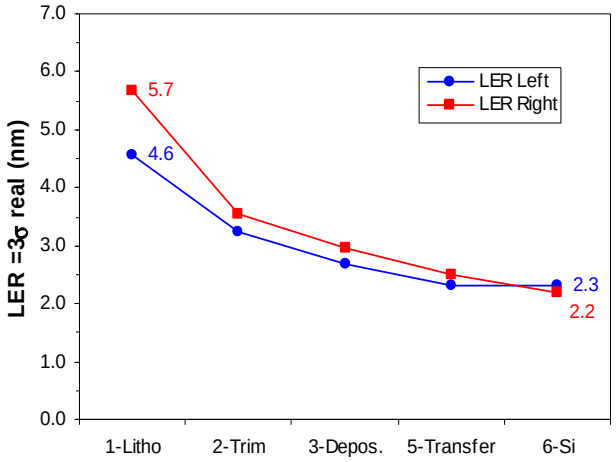

Spatial Period λ (nm)
1000
100
10
1-Litho
2-Trim
3-Depos.
5-Transfer
6-Si Etching
PSD LWR (nm3)
100
10
1
1E-3
0.01
0.1
1
Wavenumber k (nm-1)


LWR = 3σ real (nm)
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
7.5
2.5
1-Litho
2-Trim
3-Depos.
5-Transfer
6-Si
ITRS spec.
• CD = 20 nm
• LWR = 2.1 nm

LER

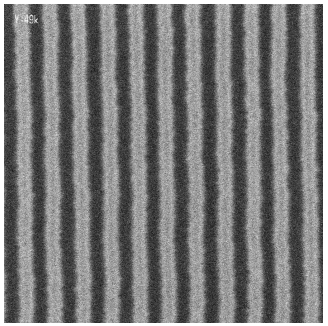



Spatial Period λ (nm)
1000
100
10
1-Litho
2-Trim
3-Depos.
5-Transfer
6-Si Etching
100
10
1
PSD LER Left (nm³)
1E-3
0.01
0.1
1
Wavenumber k (nm⁻¹)

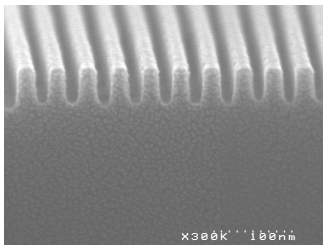

7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
LER =3σ real (nm)
LER Left
LER Right
5.7
4.6
2.3
2.2
1-Litho
2-Trim
3-Depos.
5-Transfer
6-Si

Conclusion

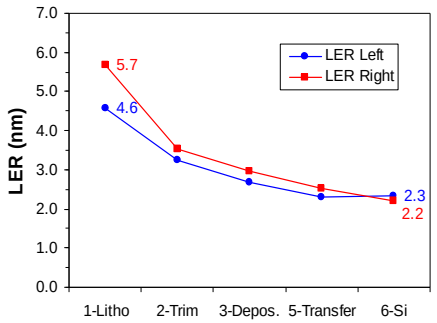
- **Demonstrated a successful integration of the resist-core spacer patterning process for 20 nm HP silicon lines**

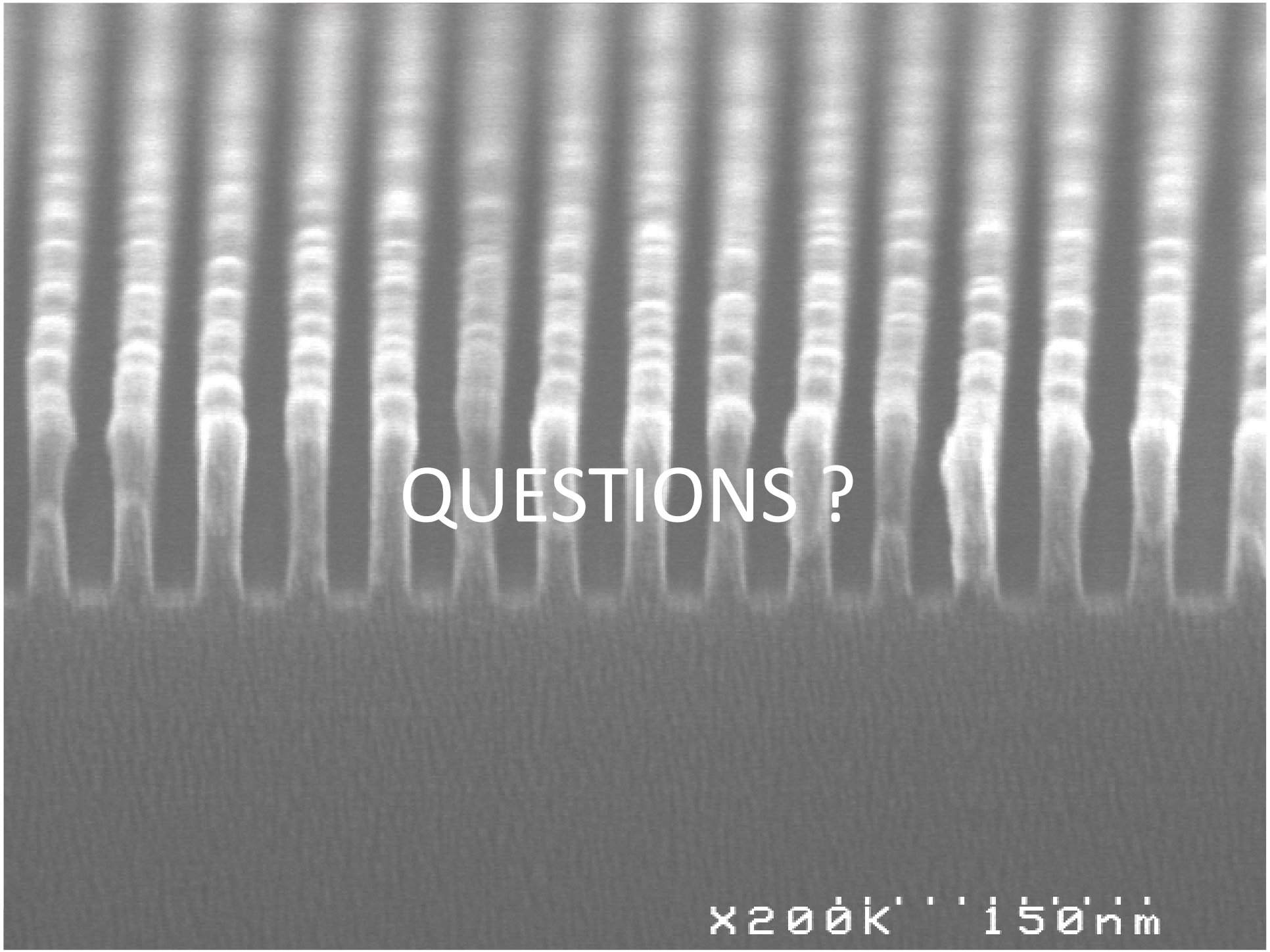


- **Full description of the sidewall roughness evolution**
  - PSD method
  - Unbiased LWR / LER measurements
  - Spectral analysis of the roughness



- **Achieved specifications**
  - L/S = 20/20 nm
  - CDU < 2 nm
  - LWR = 2.5 nm
  - LER ~ 2.3 nm




QUESTIONS ?
x200k 150nm