New plasma processes for improved dimensional control and LWR for a 28nm gate patterning

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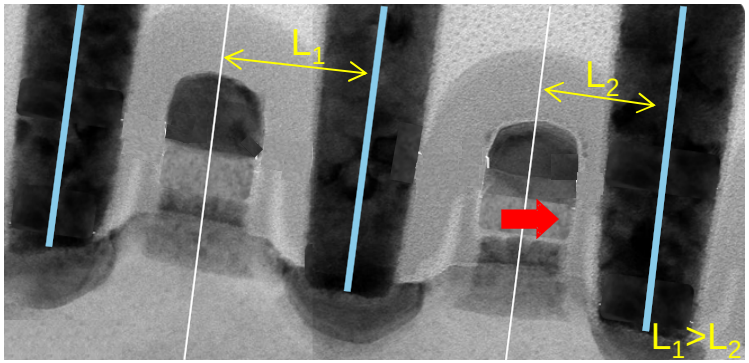
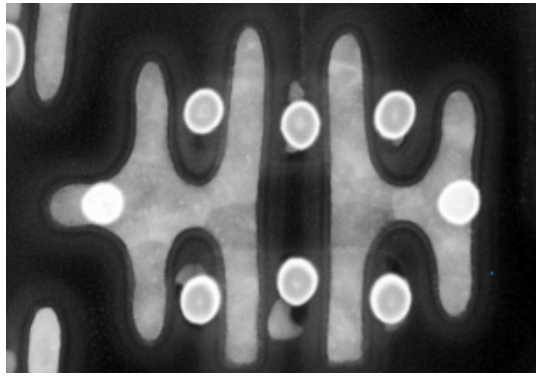
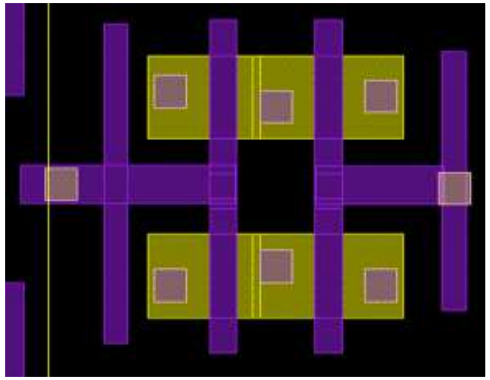
Issue description



Local OVL non-alignment of 11nm!

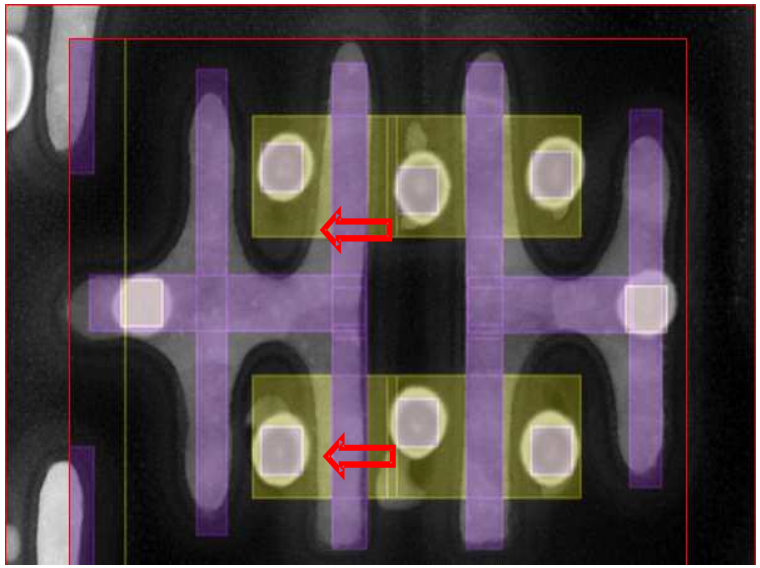


Planar deprocessing after full etch

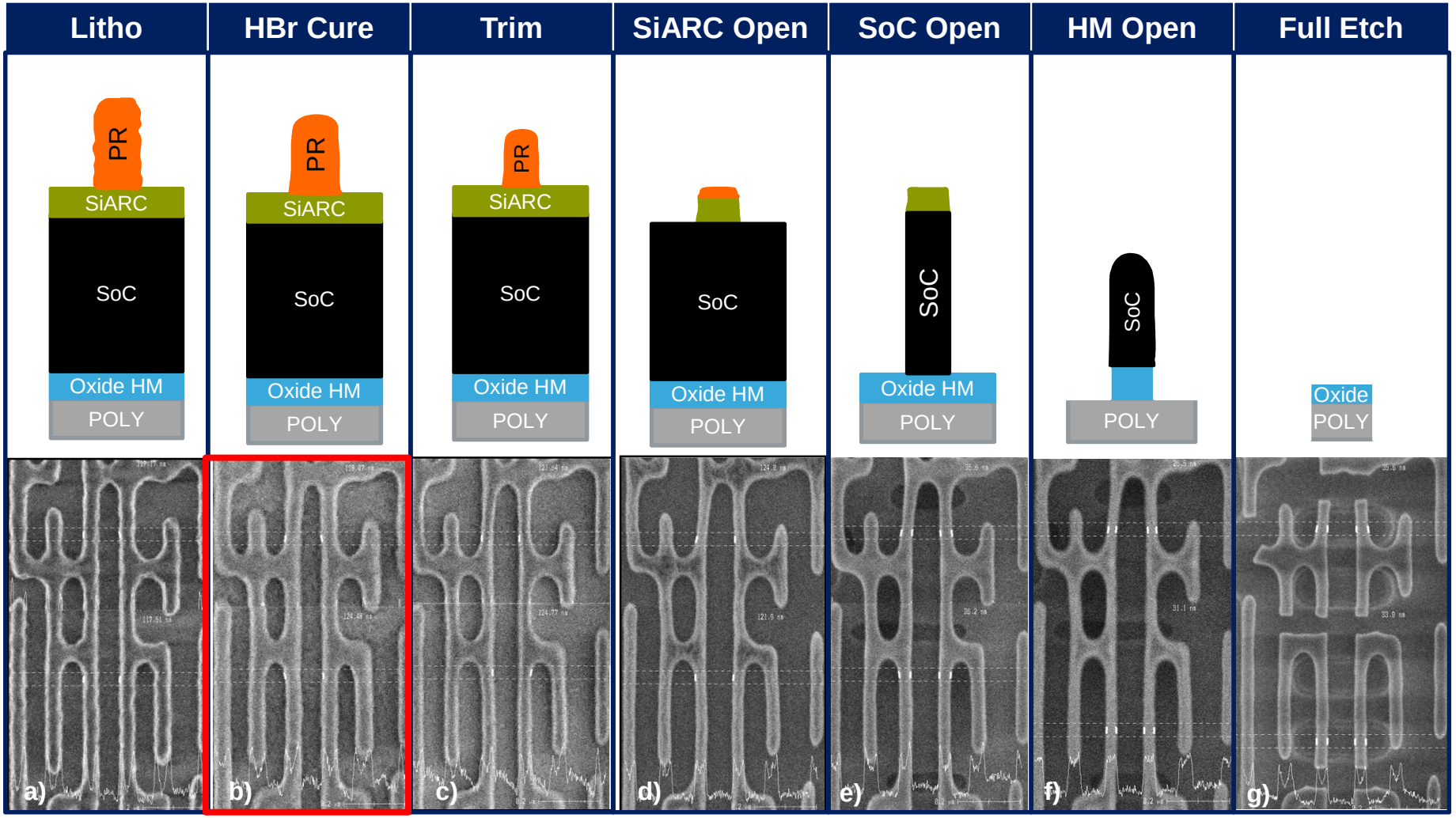


Design

Local pattern distortion is observed after gate patterning.



Gate Etch Process Partitioning



The cure step has been identified as a root cause for Gate Shifting

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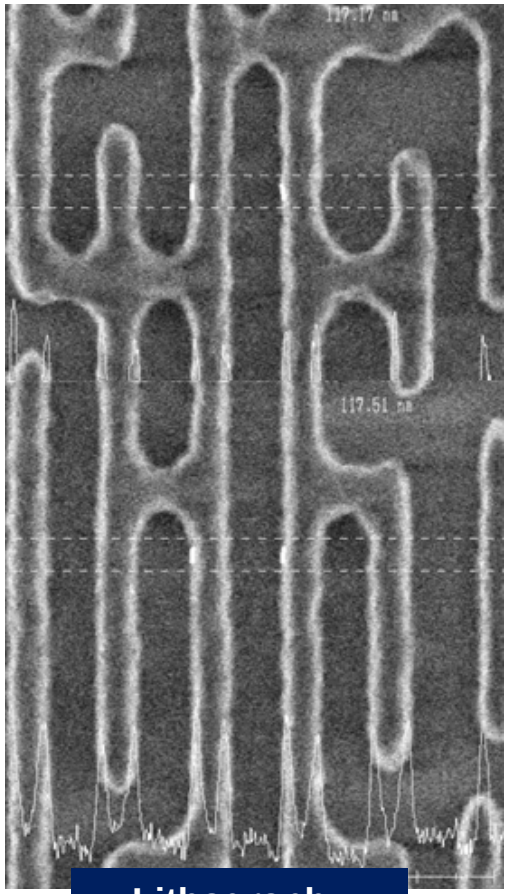
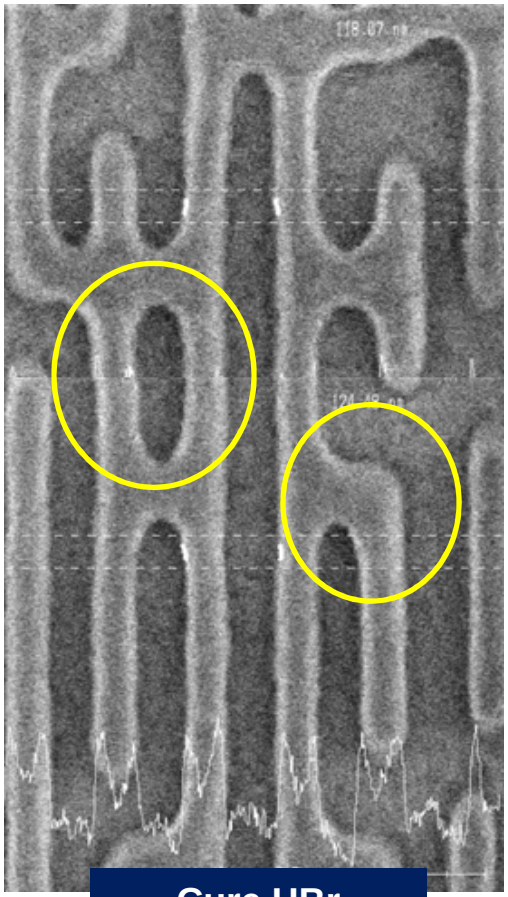
Pattern shifting

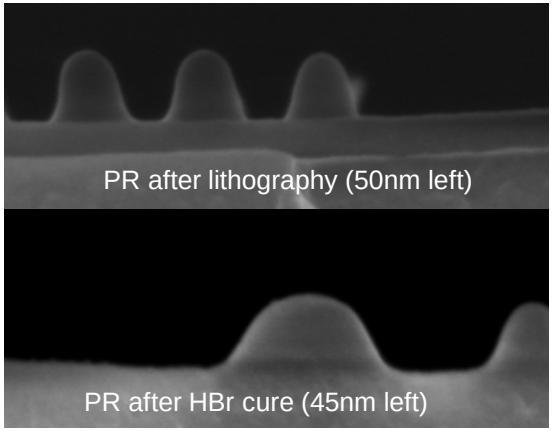


Lithography



Cure HBr

Cure step leads to polymer degradation and leads to an overall resist flowing.



SEM Xsection (by LAM research)

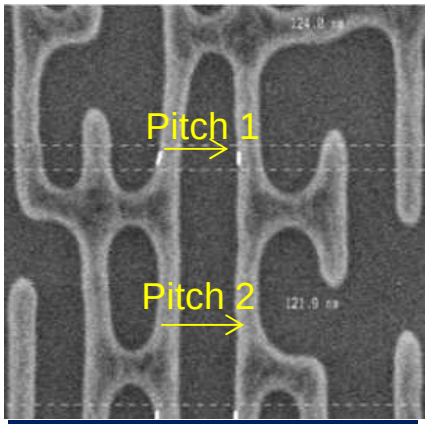
The resist reflow during HBr cure is responsible of gate shifting.

New challenge → Pattern shifting

Pattern Transfer
SiARC etch without Cure

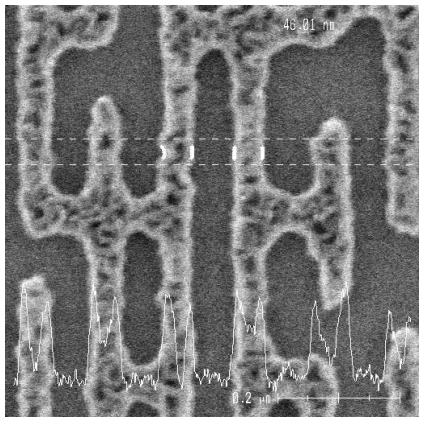
Cure step removal allows to maintain respectable Gate shifting but increases LWR

Pictures after SiARC open



With HBr Cure

Low LWR~3.5nm
High Gate Shift~4,5nm



Without HBr Cure

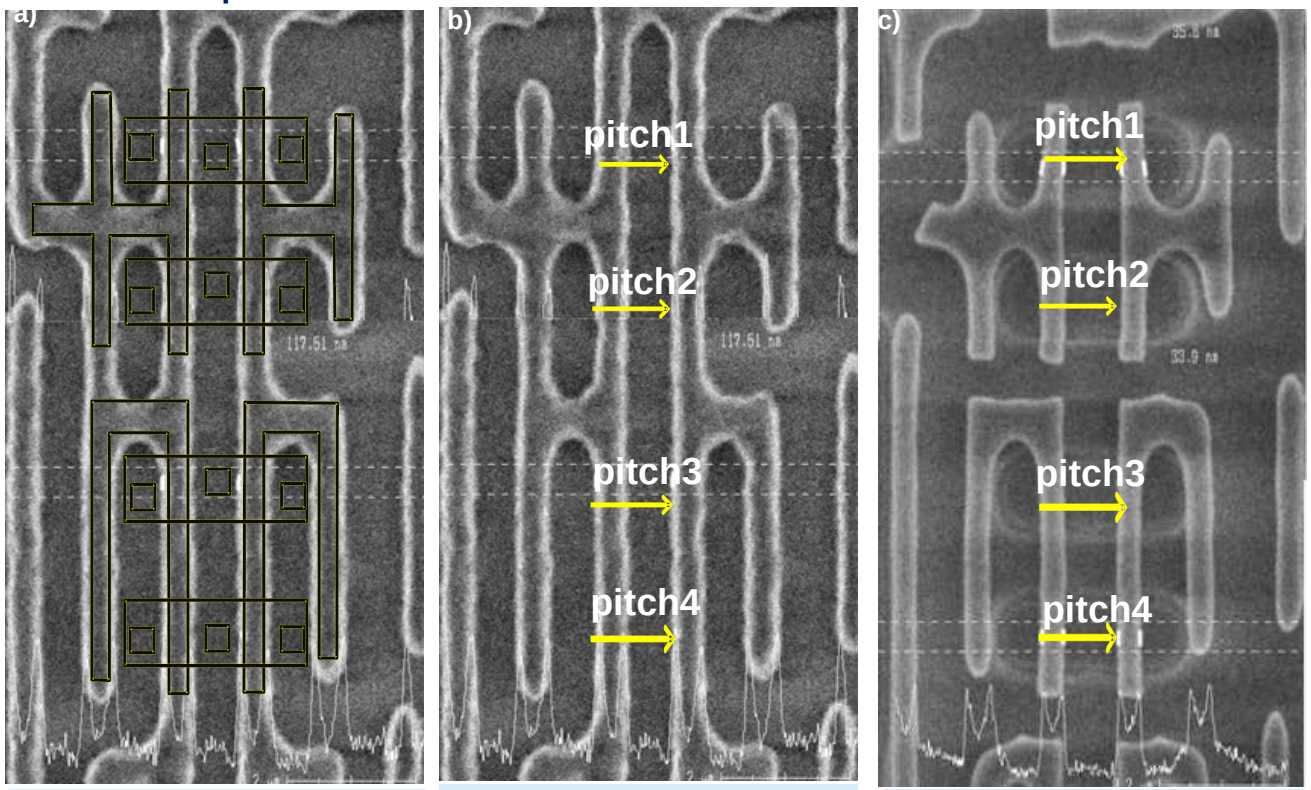
High LWR~11,8nm
Low Gate shift ~0,5nm

A compromise have to be found to control both Gate shifting and LWR.

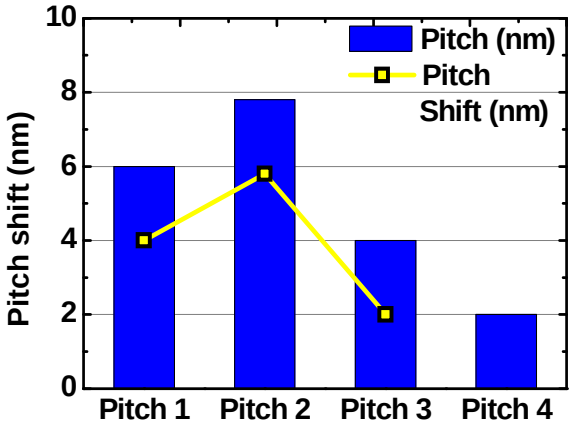
We will focus over SiARC etching process and subsequent pattern transfer steps

Metrology issue

Pitch = CD+Space



Design | **Lithography** | **Full Etch**

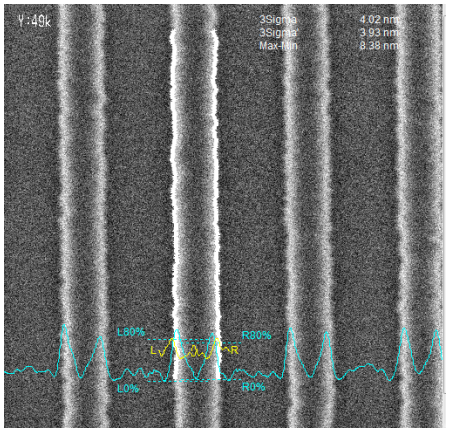


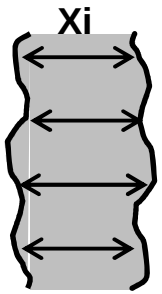
Pitch 4 remains stable after etch while Pitch 2 is increased.

Pitch 2 shift is a signature of pattern shifting from initial design.

Two methods for LWR

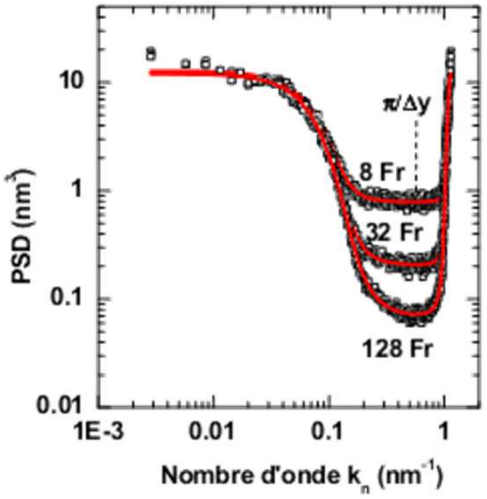
CD-SEM



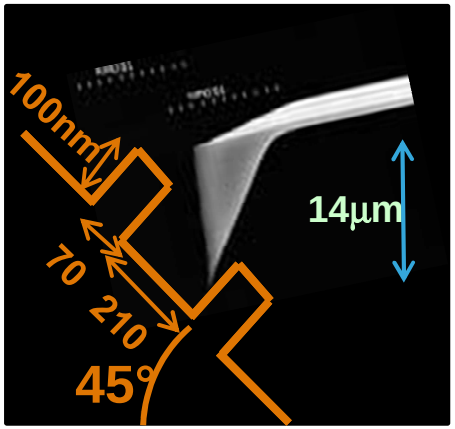


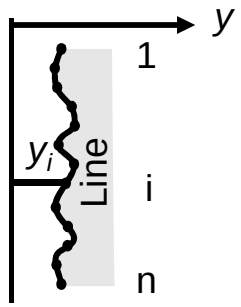
LWR = 3 x stdev(CD)

- **Top view observations**
- **LWR and LER**
- **Allows spectral analysis**



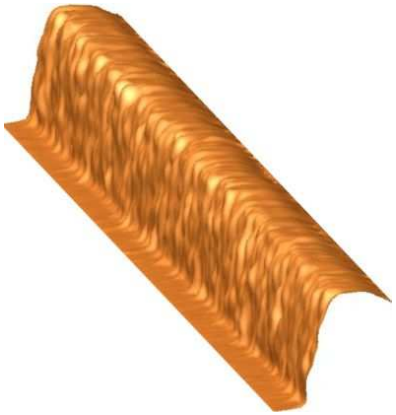
Tilted AFM



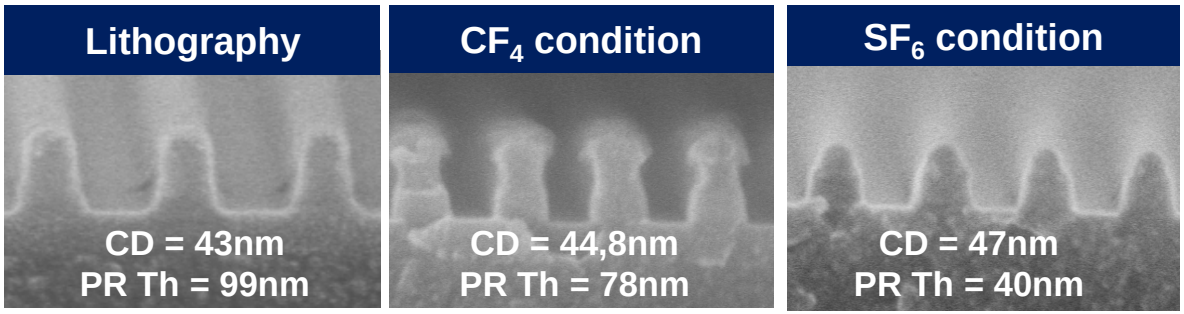


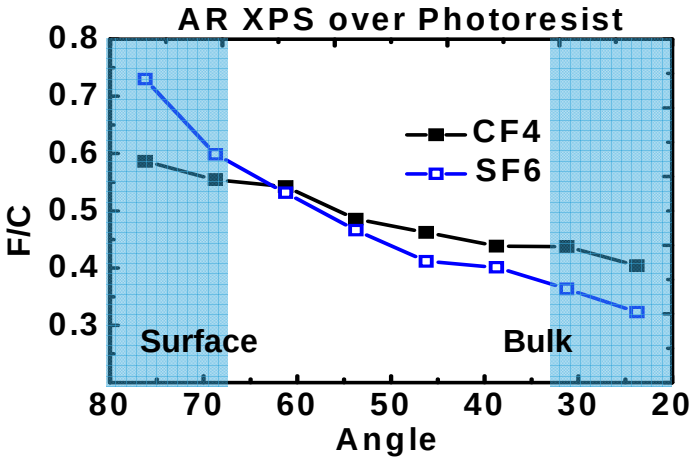
LER = 3 x stdev(y)

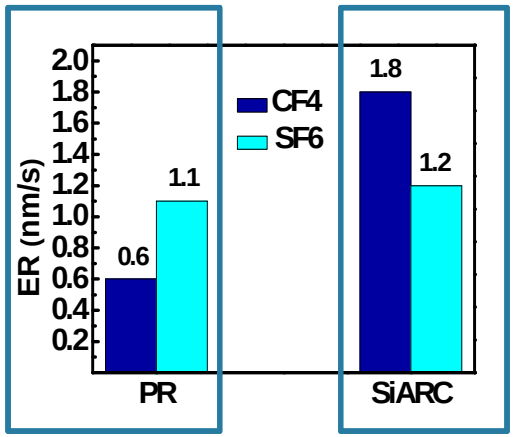
- **Only for LER**
- **Half profile scanning**
- **Estimation of LER all along the pattern height**

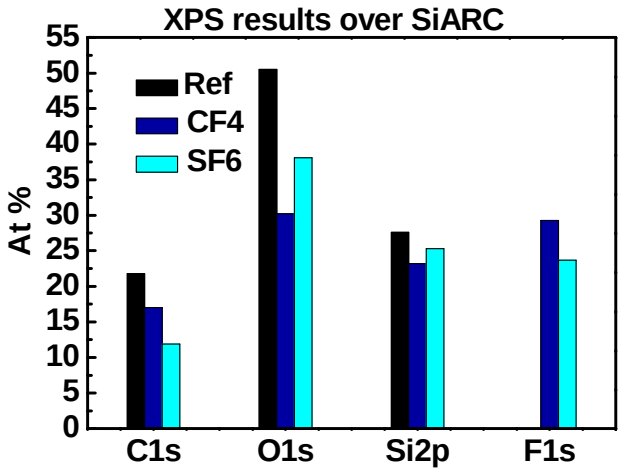


Comparison of SiARC plasma etching processes









A C-rich surface layer in CF4 decreases PR ER and increases LWR.

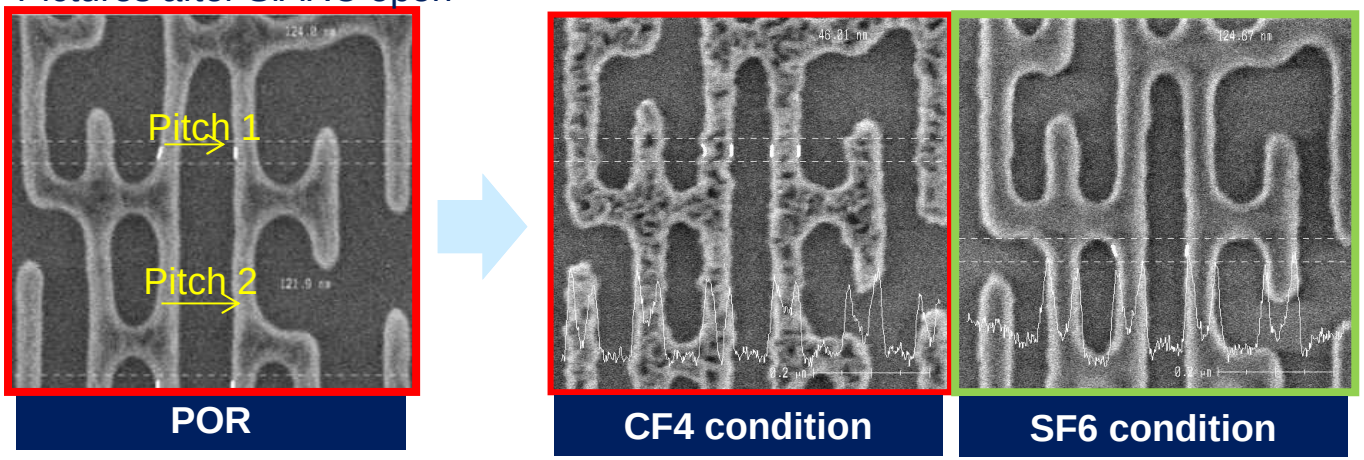
F-rich surface layer in SF6 increases PR ER and trims PR smoothing the surface.

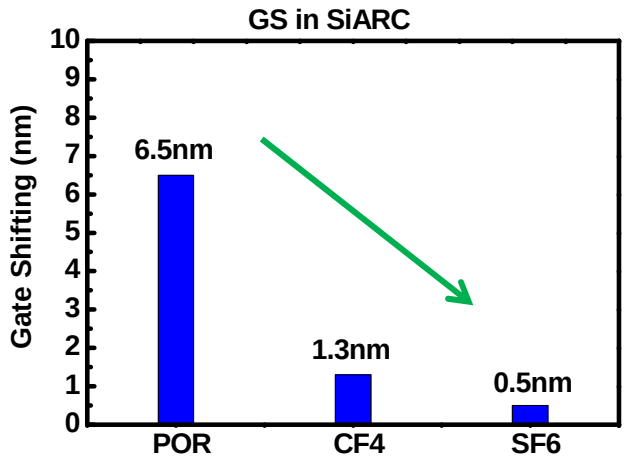
SiARC ER is higher in CF4 due O depletion by Carbon

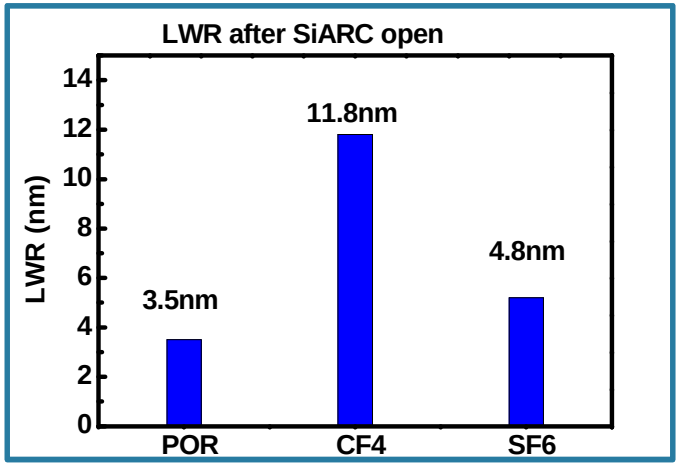
Pattern Transfer
SiARC etch without Cure

New process in SF6 was proved to improve Gate Shifting and LWR

Pictures after SiARC open







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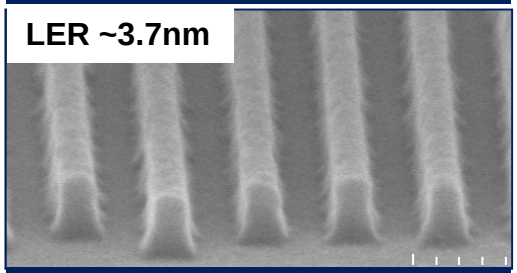
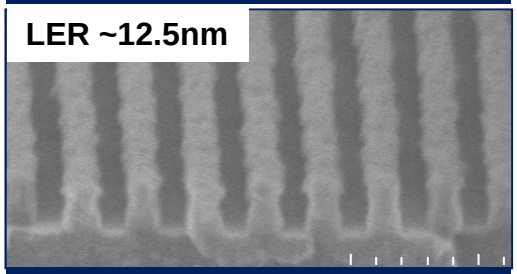
Study of Roughness over Photoresist

CD-SEM Measures

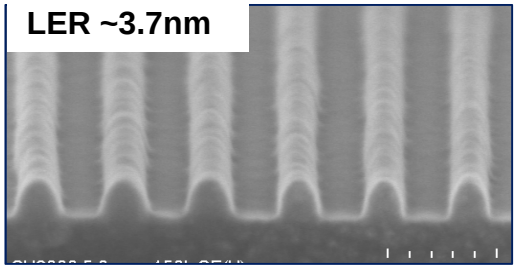
Lithography

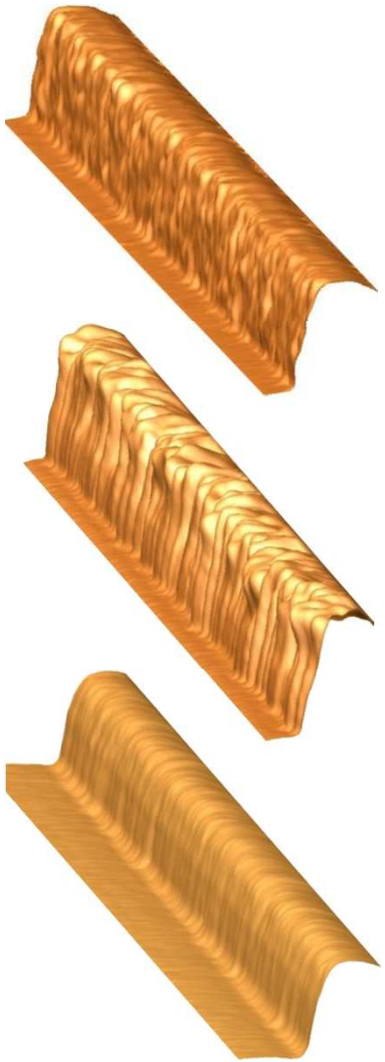


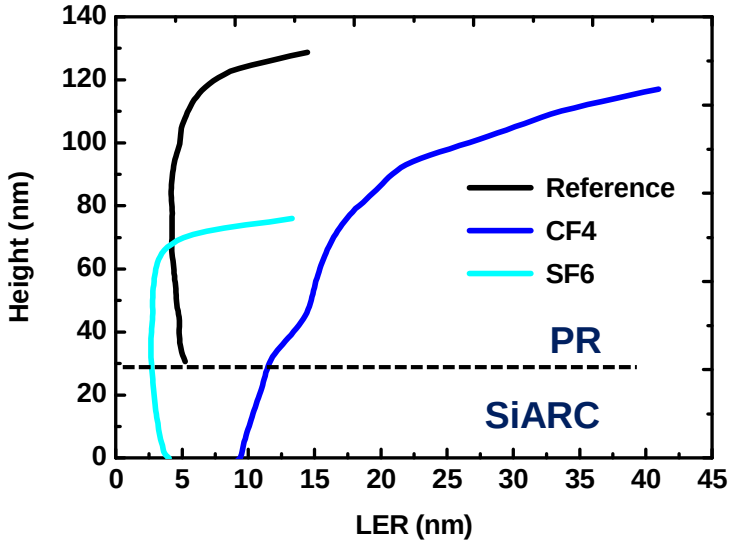
CF_4 condition



SF_6 condition







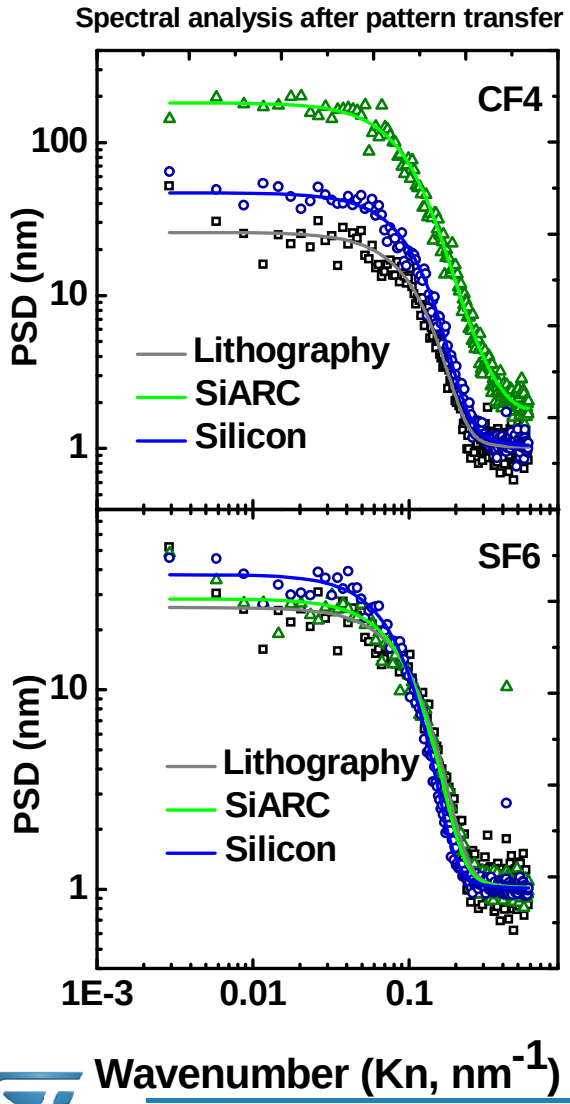
LER PR	4.5nm
LER SiARC	-

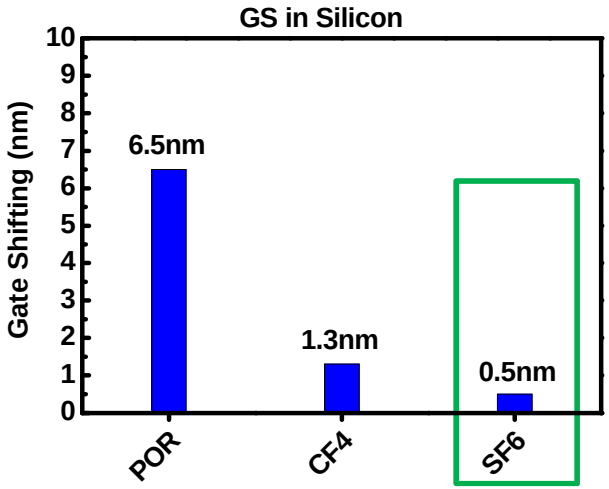
In CF4 photoresist LWR is degraded during process and partially transfered into SiARC.

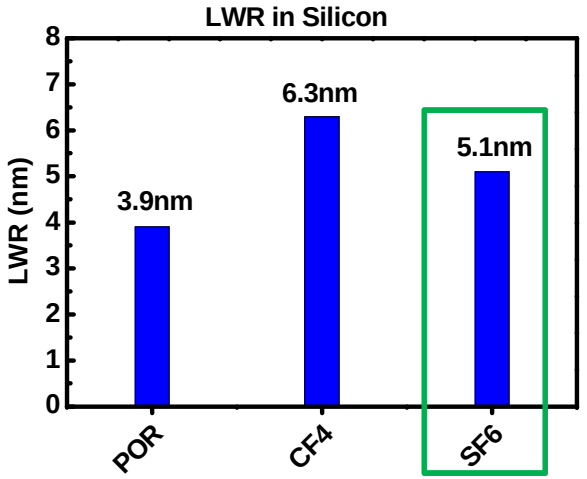
In SF6, F rich surface layer will trim the photoresist and smooth it during transfer.

Resulting LER is better in SF6 plasmas

Roughness transfer into Silicon







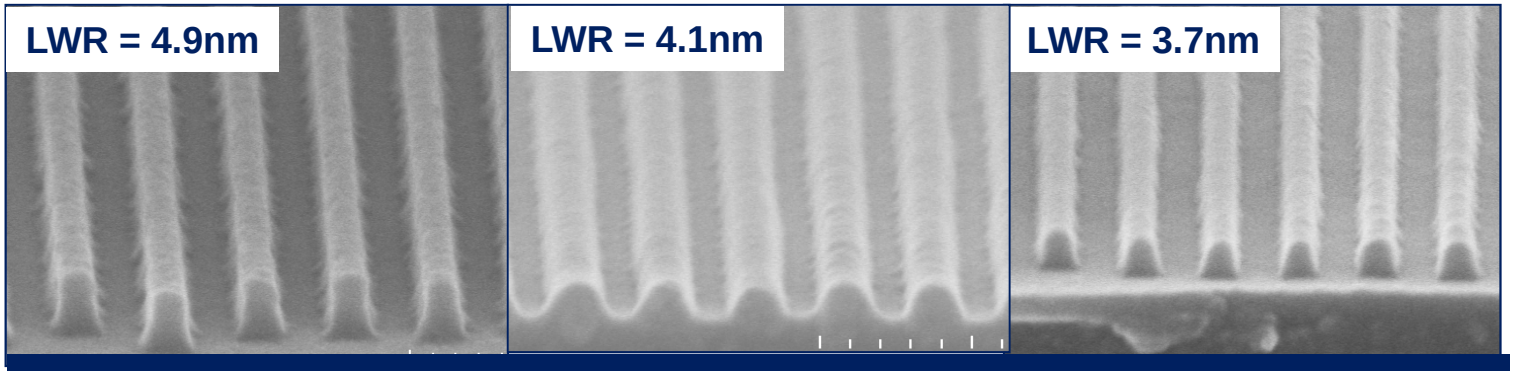
After transfer to Silicon, SF6 plasma is the best option for LWR and GS decrease

In CF4 all roughness frequencies are increased but during pattern transfer just low frequencies are transferred, leading to high LWR.

Spectral analysis of LWR in SF6 does not show roughness improvements since lithography value is underestimated. Despite subsequent gate etch steps degrade LWR.

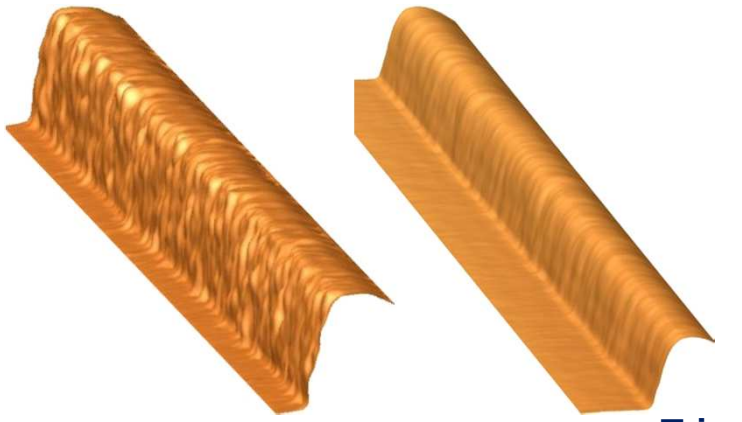
How to improve LWR?

Measures over Photoresist



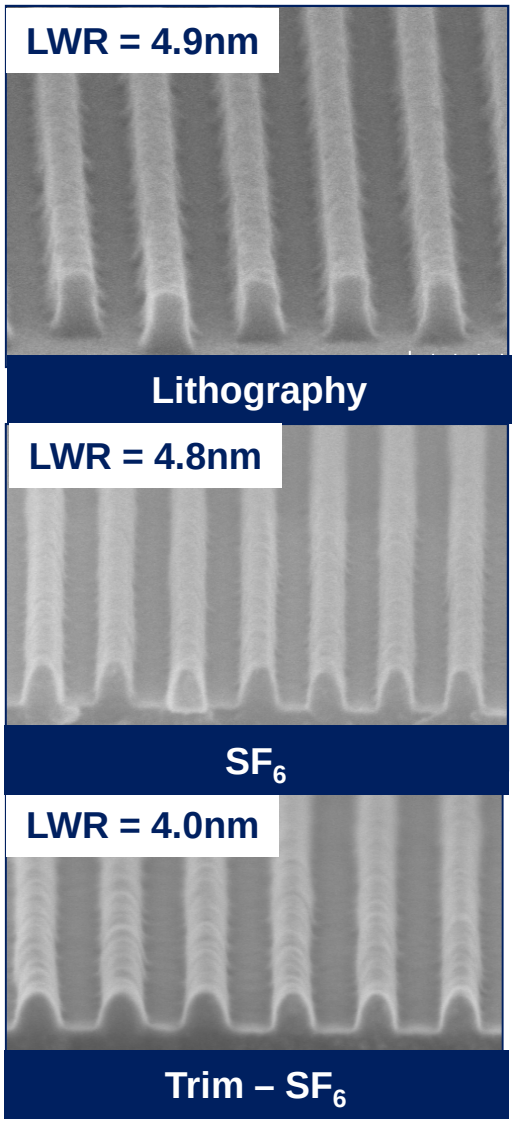
	Lithography	HBr Cure	Trim
GS	1.0nm	6.0nm	1.4nm
LER	4.4nm	3.0nm	2.2nm

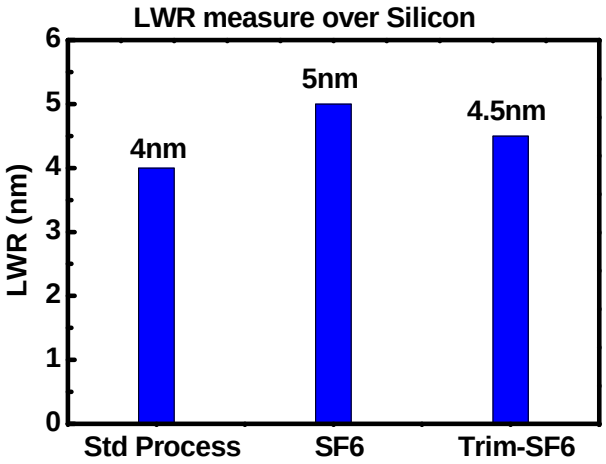
Photoresist trim has been identified as a good option to limit LWR without Gate Shifting.

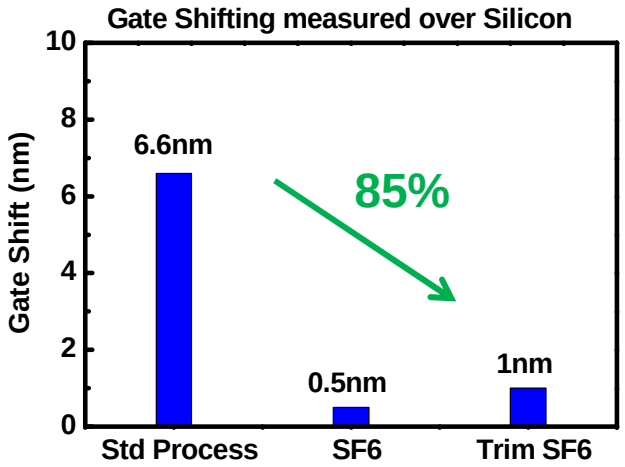


Trim steps to correct LWR

Measures over SiARC







LWR measures taken over SiARC show a big roughness improvement with Trim step addition.

Measures after transfer to Silicon prove that Gate shifting will not be degraded during gate etch but LWR can be degraded due to subsequent etch steps.

Conclusion

- Cure steps improve LWR but distort gate patterns.

→ Cure step removal requires new plasma processing for gate patterning.

- A new SiARC etching process in SF6 has been compared to the standard process in CF4

→SiARC etching in CF4 leads to C-rich hard surficial layers that increase LWR

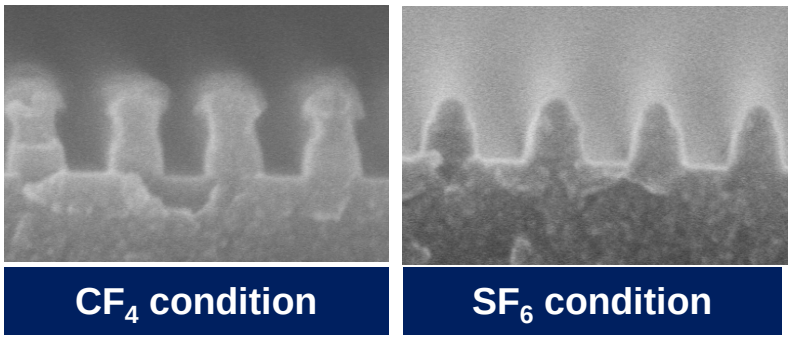
→SiARC etching in SF6 leads to F-rich reactive layers triming photoresist and resulting in lower LWR.

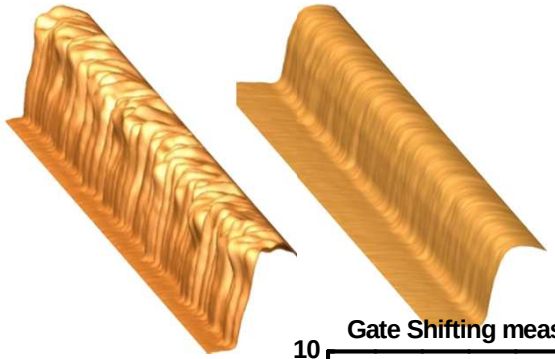
- AFM gate profile analysis shows that LER is lower in SiARC than in Photoresist.

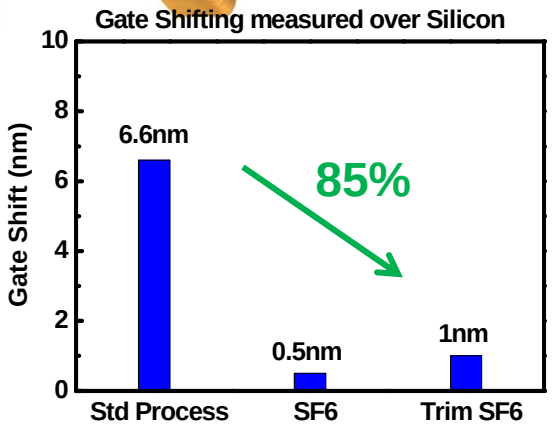
- Spectral analysis of LWR transfer for these two plasmas shows a degradation of LWR during gate etch processing.

- Addition of Trim steps has been proved to reduce initial LWR

→ New process Trim-SF6 allows GateShifting improvement of a 85%







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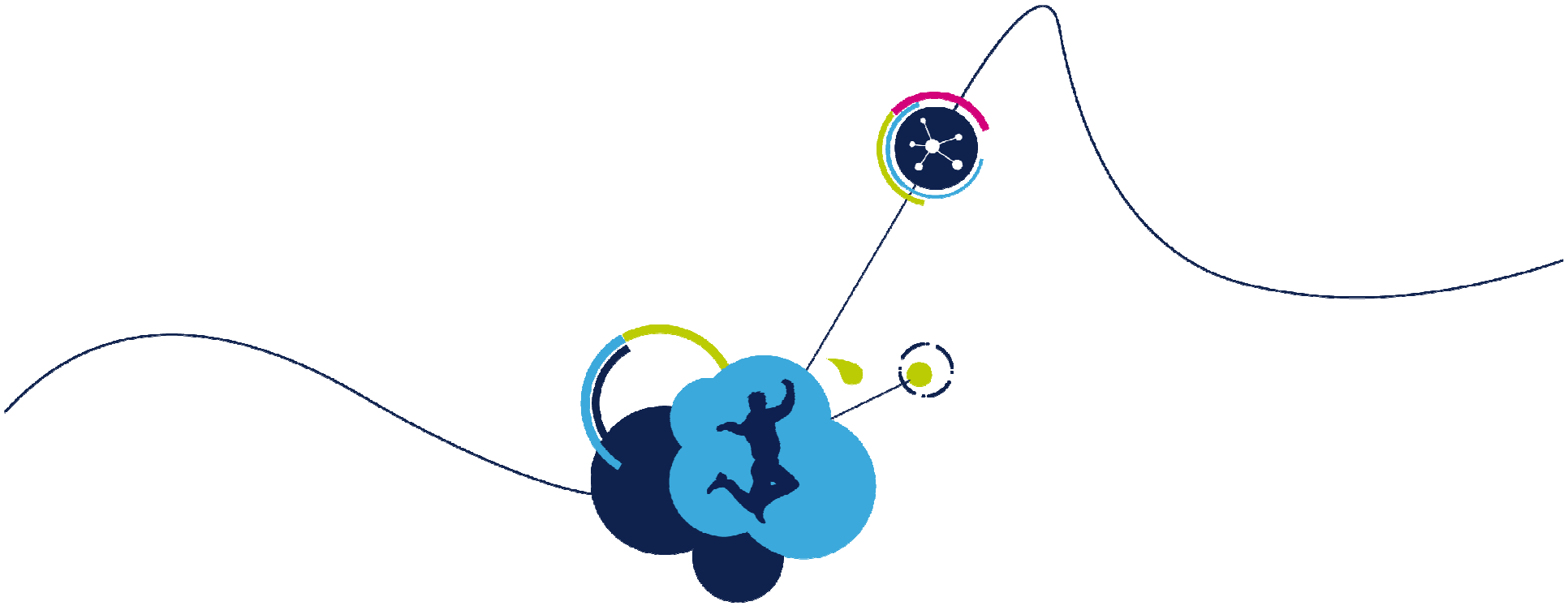

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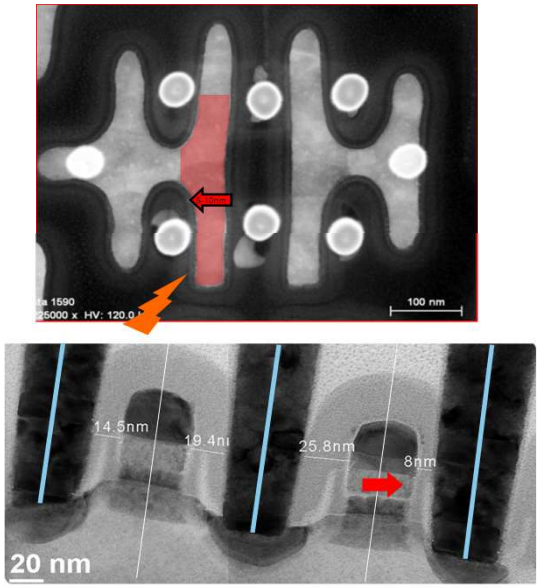
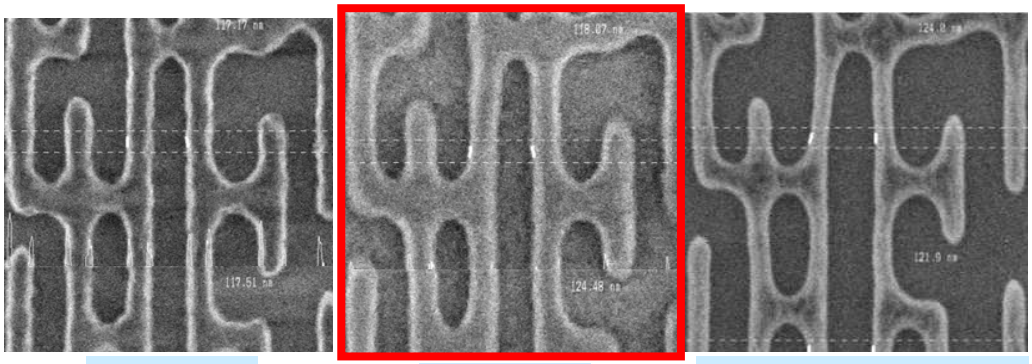
How to solve it?

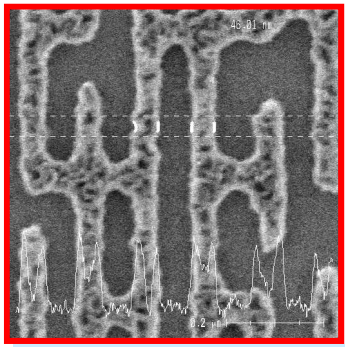
Gate shifting has an impact on the electrical performance of the device.



The cure step is mandatory to ensure minimized gate LWR but it is the main contributor to pattern shifting.



LITHO **CURE** **Trim PR+SiARC**

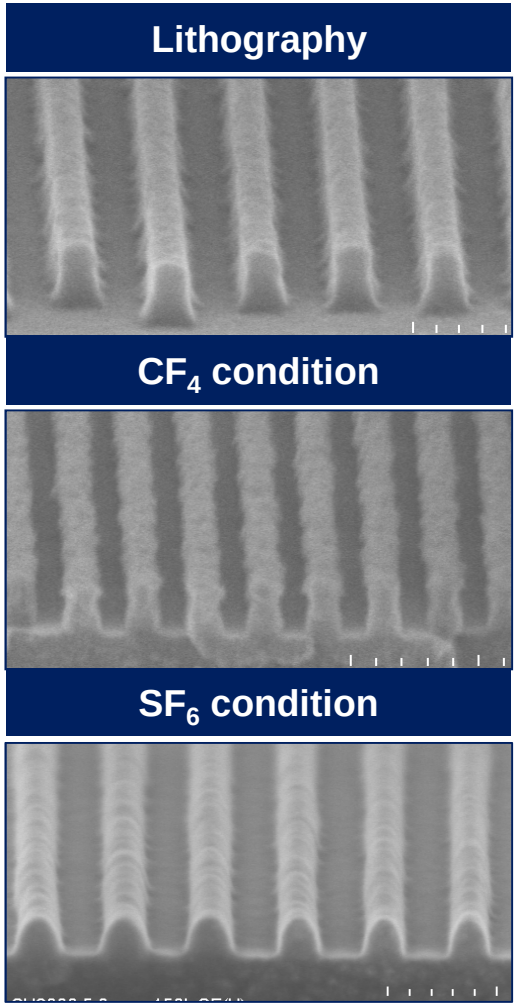


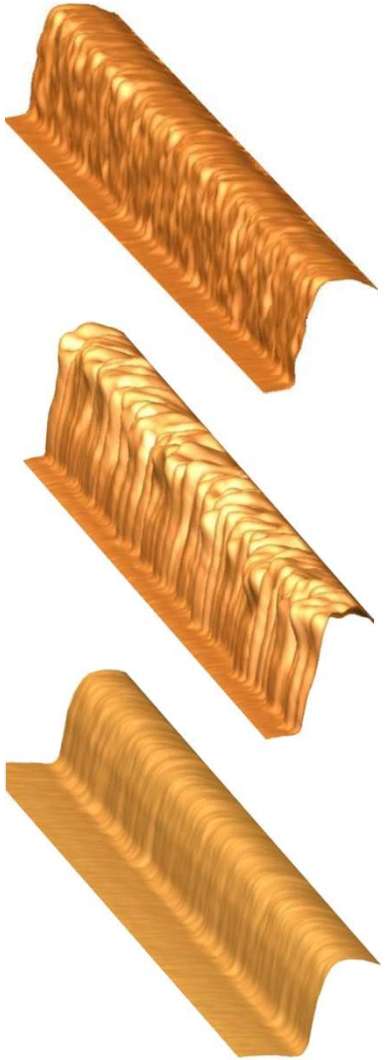
SiARC wo CURE, wo TRIM

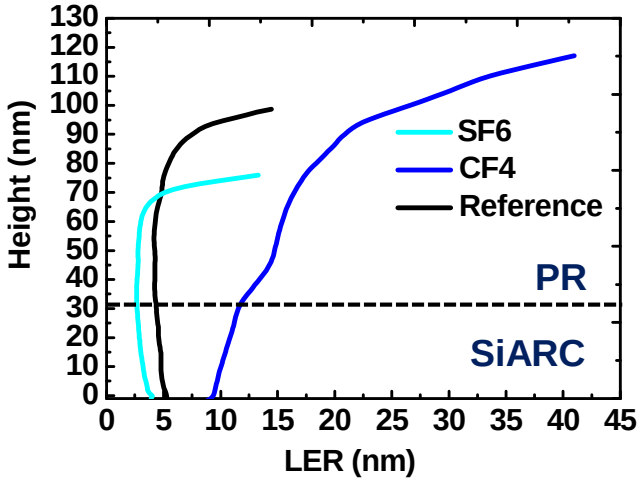
New strategies have to be implemented to fulfill the requirements of the 20nm technological node in terms of LWR and gate shifting:

1. **Optimization of the hard mask opening steps (Si ARC etching and trim, SOC and TEOS etching)**
2. **Optimization of the cure step**

Study of Roughness over Photoresist







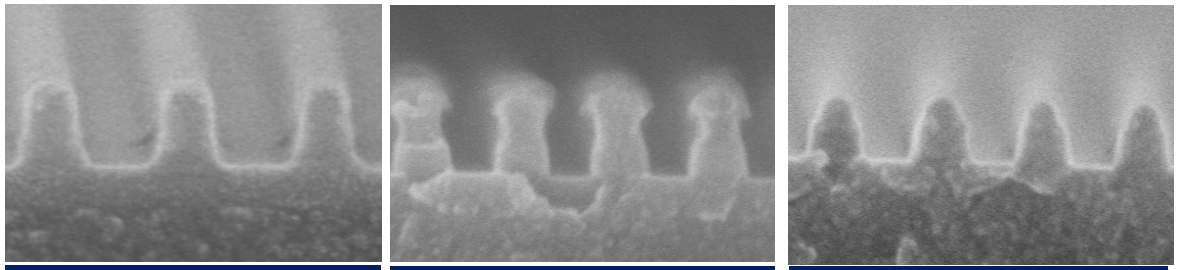
LER PR	4.5nm	15.2nm	2.7nm
LER SiARC	-	10.9nm	2.8nm

In CF4 initial PR roughness is partially transferred into SiARC sidewalls.

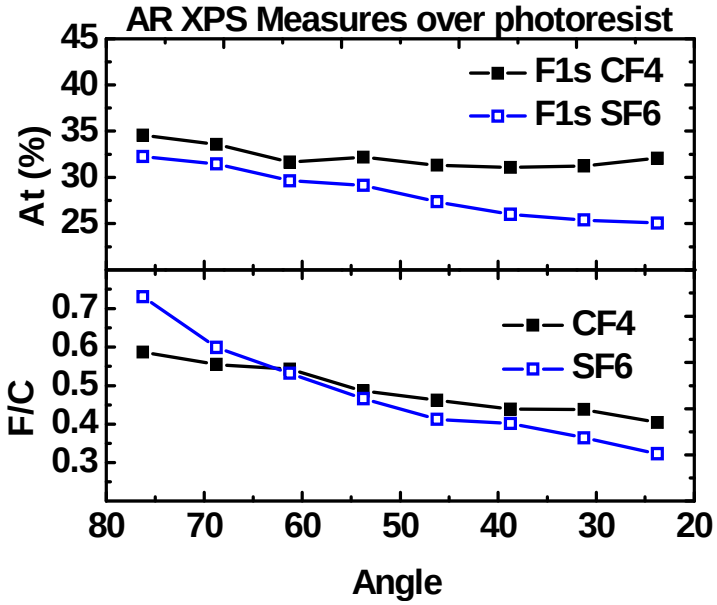
In SF6, initial PR roughness is smoothed during SiARC opening.

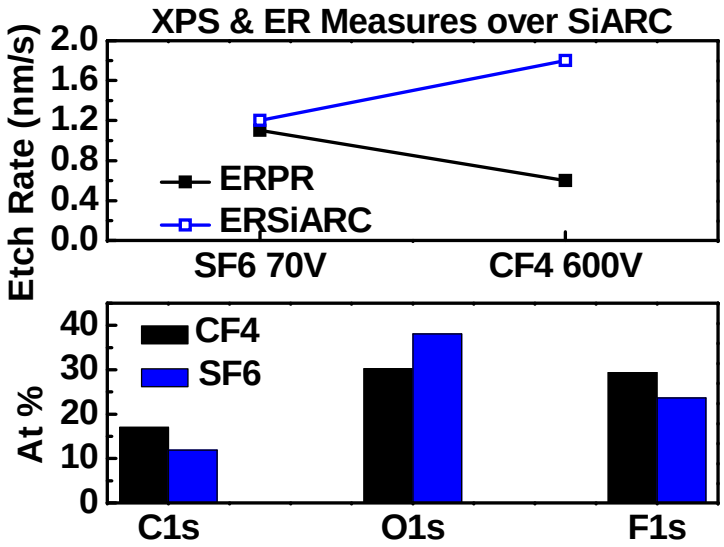
Resulting LER is better in SF6 plasmas

Comparison of SiARC plasma etching processes



Lithography	CF_4 condition	SF_6 condition
CD = 43nm PR Th = 99nm	CD = 44,8nm PR Th = 78nm	CD = 47nm PR Th = 40nm





A C-rich hard surface layer is deposed in CF4 plasmas that prevents photoresist etching and increases LWR.

In SF6 plasmas a F-rich surface layer increases photoresist etch rate and LWR is not impacted.

SiARC ER is higher in CF4 due to a higher C and F content that will increase Oxygen depletion and Si Etch