



ETCH DEVELOPMENT FOR E-MODE GaN POWER HEMT FABRICATION

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BACKGROUND



GaN has a wide band gap:

3.4 eV vs 1.1 eV for Si

GaN has a higher e- mobility:

2000 vs 1450 (cm²/V-sec) for Si

GaN is **quite inert** and **wet etching is limited**

Applications:

- consumer electronics
- telecommunication
- AC/DC converters
- solar/wind power systems

Why GaN instead of Si ?

- High electron velocity
→ devices @ **high speed**
- High breakdown field
→ devices @ **high voltage**
- High thermal conductivity
→ devices @ **high temperature**

OUTLINE

- ❑ background GaN etch
- ❑ GaN high power transistor
- ❑ concept 1: MISHEMT
 - Controlled barrier recess: concept + results
- ❑ concept 2: pGaN HEMT
 - Selective pGaN/AlGaN etch: concept + results
- ❑ Conclusions

BACKGROUND

- GaN ETCH

Bond Strength	
Ga-Ga	33+-5 kcal/mol
Ga-O	14.7eV
Ga-N	8.9 eV
Ga-As	6.5 eV
Al-N	11.52 eV
Al-O	21.2 eV
In-N	7.72 eV

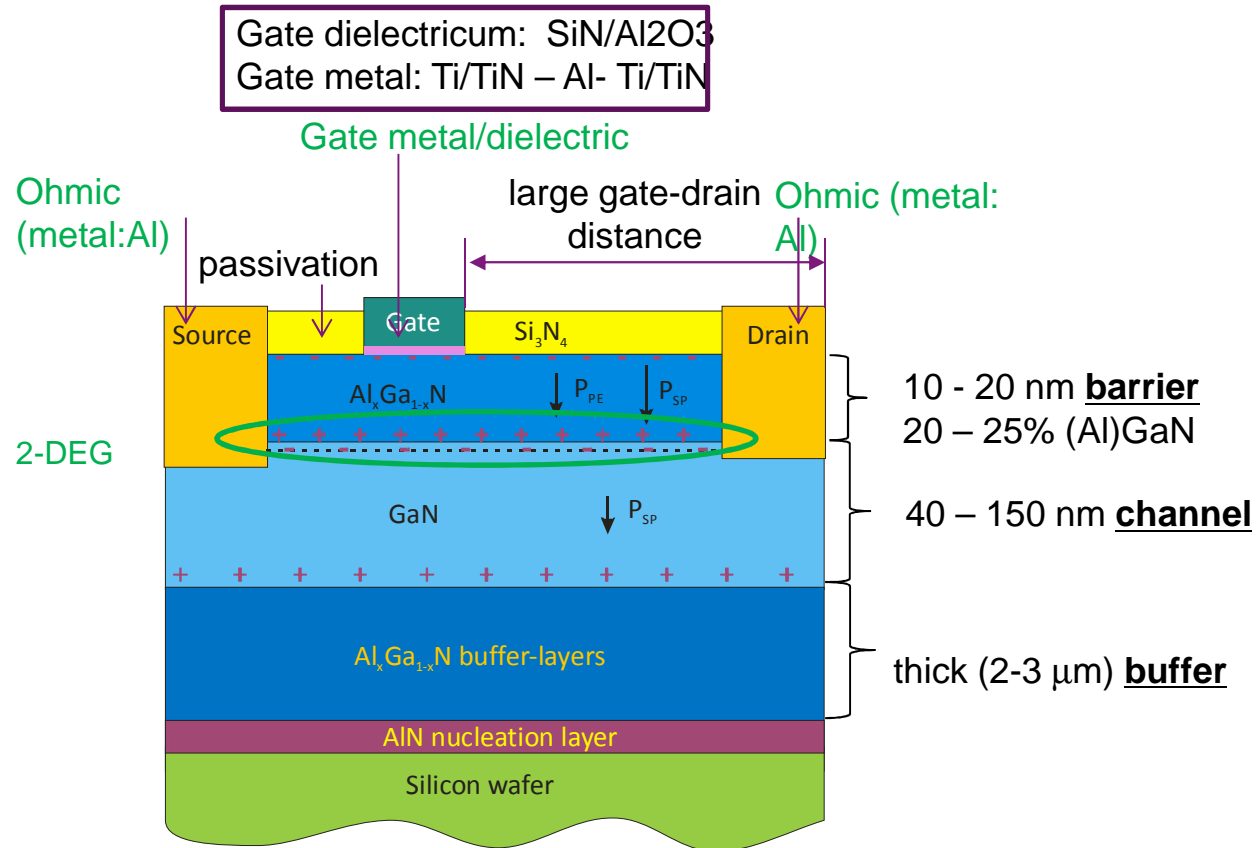
- Bond strength:
Ga-O/Al-O >> Ga-N
→ Important for selective etch

	Bp- C	H2O solubility
GaBr3	278.8	soluble
GaCl3	201.3	very soluble
GaCl2	535	decomposes
GaF3	Subl . 800C	Insoluble
Ga2H6	D> 130	decomposes
Ga2O3	-	Insoluble
(CH3)3Ga	55.8	

- GaCl₃ mainly formed during etch:
→ GaCl₃ more stable than GaCl₂
- GaF₃ is very non-volatile

Etch tool: LAM Versys2300 TCP (ICP) reactor

GaN POWER (E-MODE) TRANSISTOR - ZOOM IN

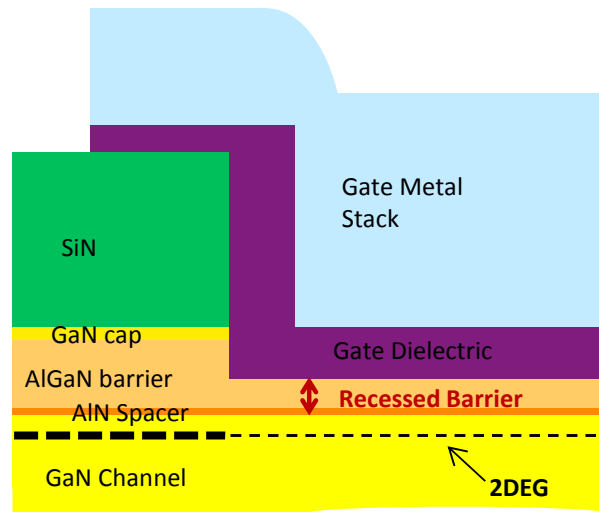


HEMT: High Electron Mobility transistor

MISHEMT: Metal-Insulator-Semiconductor High Electron Mobility Transistor

CONCEPT 1: MISHEMT

Concept 1: Barrier Recess



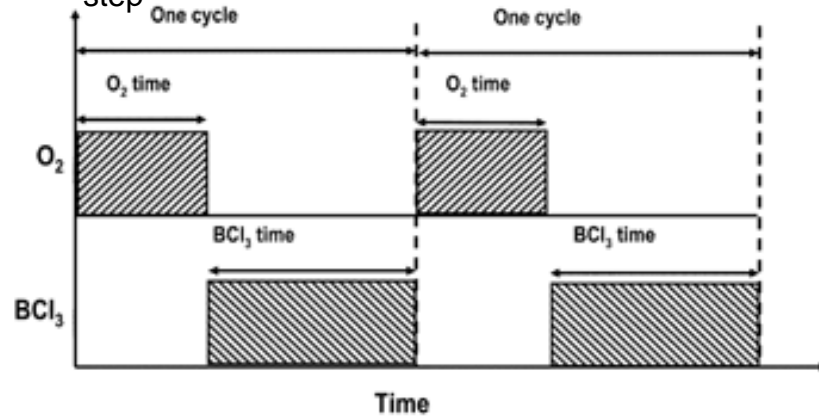
Principle: **suppressing 2-DEG formation** below gate area by **recessing the barrier**
→ E(nhancement)-mode device if $V_{th} > 0$ is applied to the gate electrode

Etch requirements:

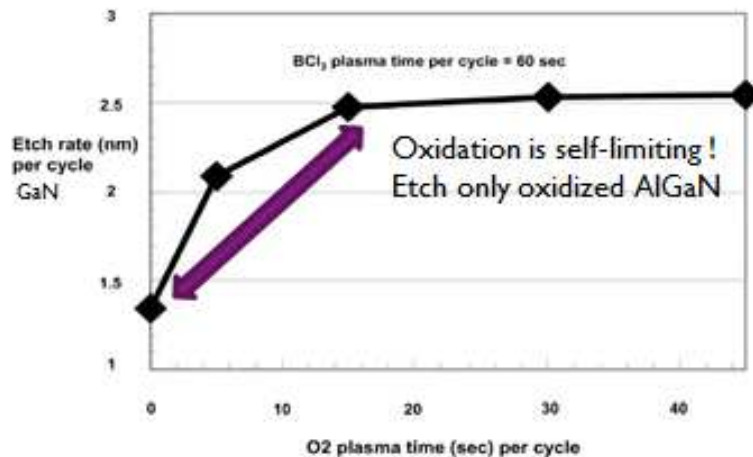
- Very low/controllable AlGaN barrier etch rate
- Minimal surface roughness
- Clean Surface
- Low non-uniformity

CONTROLLED BARRIER RECESS - ALE (ATOMIC LAYER ETCH)*

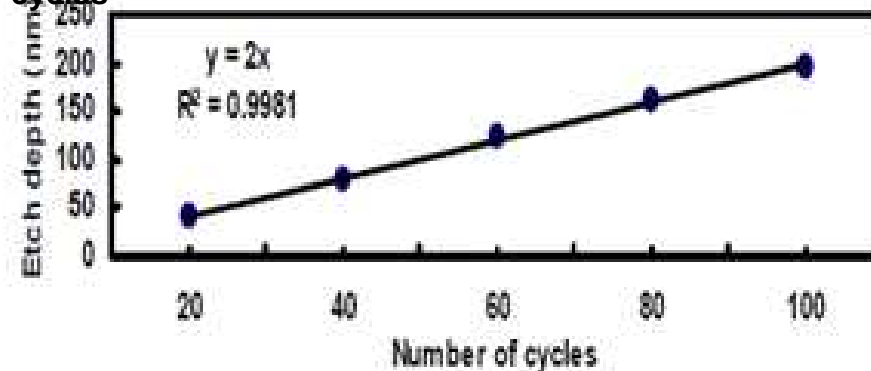
Alternating self-limiting oxidation and etch step



- BCl₃ etches oxidized AlGaN almost 2 times faster than the non-oxidized layer.
- GaN and AlGaN etches substantially identically because the Al does not prevent the oxidation or the etching by BCl₃.
- The thickness of the oxide layer in the AlGaN/GaN material depends on the plasma power used to oxidize the material.



Linear behaviour of the ALE etch depth vs. number of ALE cycles

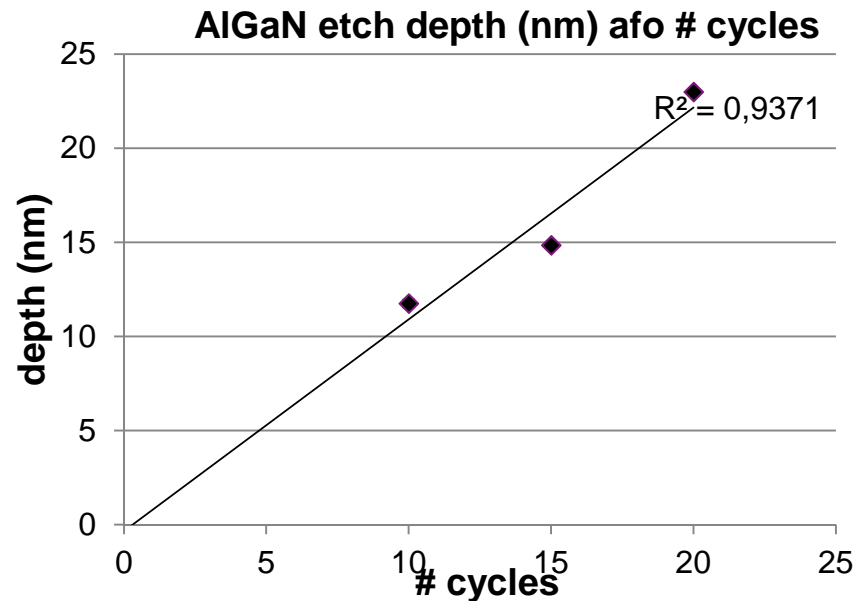
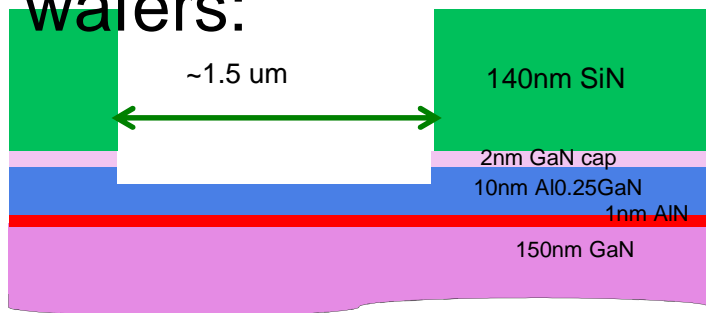


*reference: [US patent 8.124.505](#): Two stage plasma etching method for E-mode GaN HFET

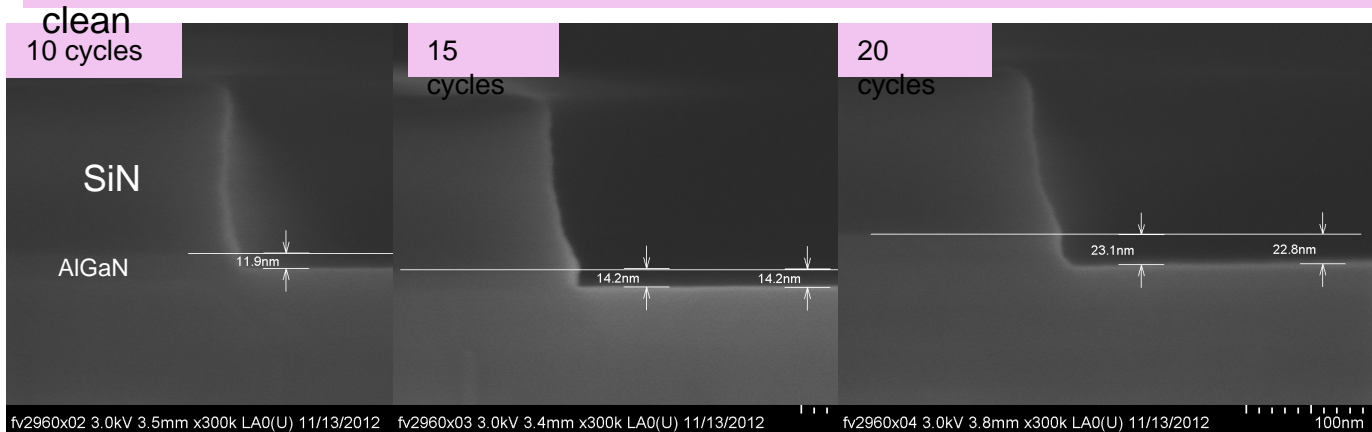
CONTROLLED BARRIER RECESS

- RESULTS

Test wafers:

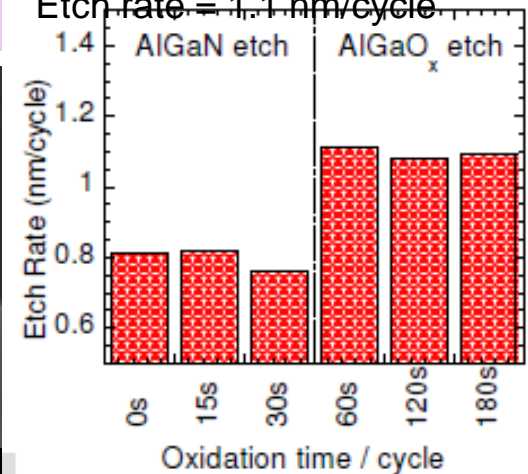


SiN etch (SF₆) + PR strip + #cy(90" oxidation (O₂) / 30" BCl₃ etch) + wet

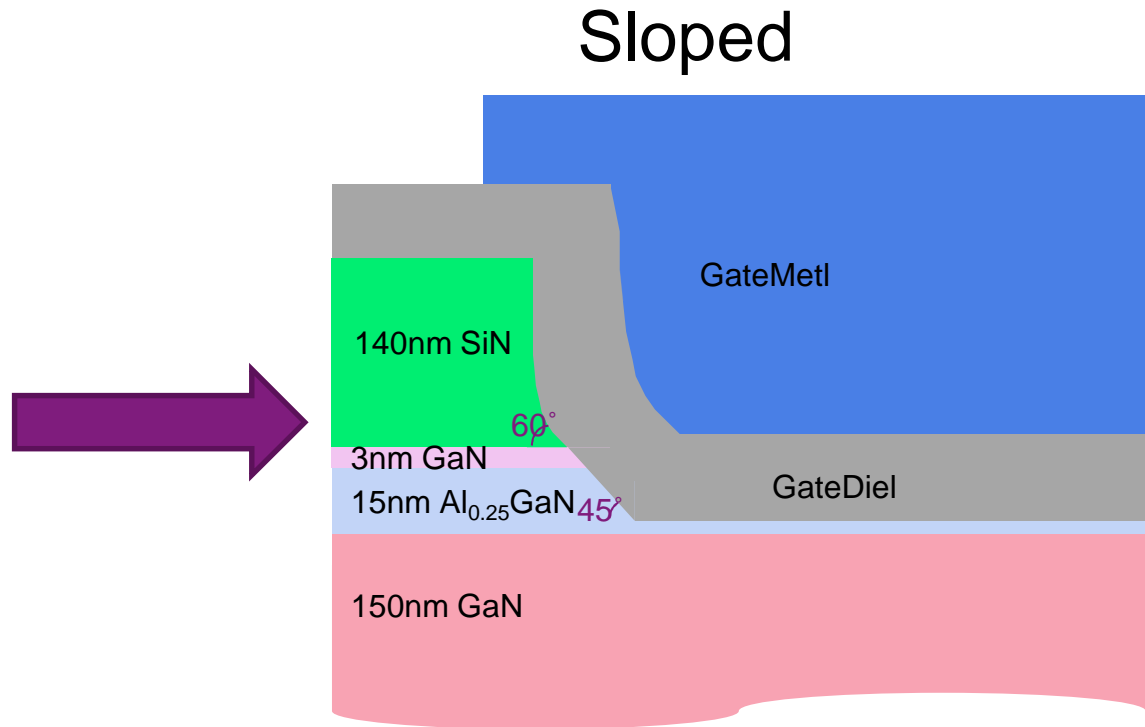
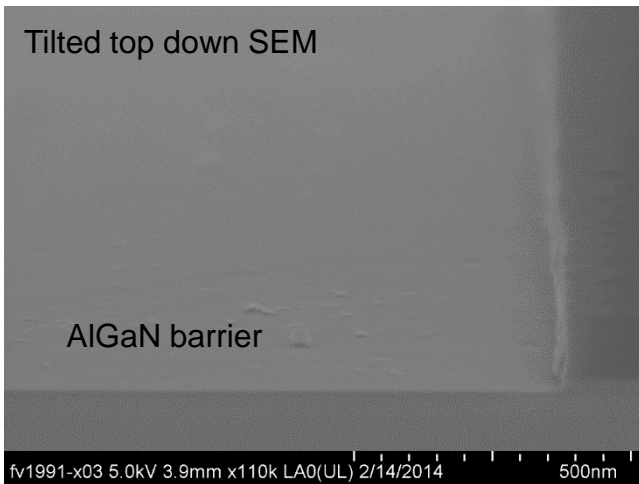
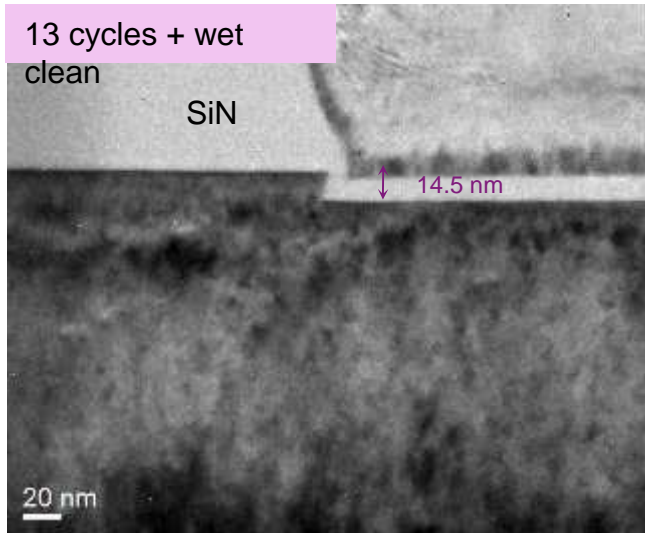


Minimum oxidation time = 60 s

Etch rate = 1.1 nm/cycle



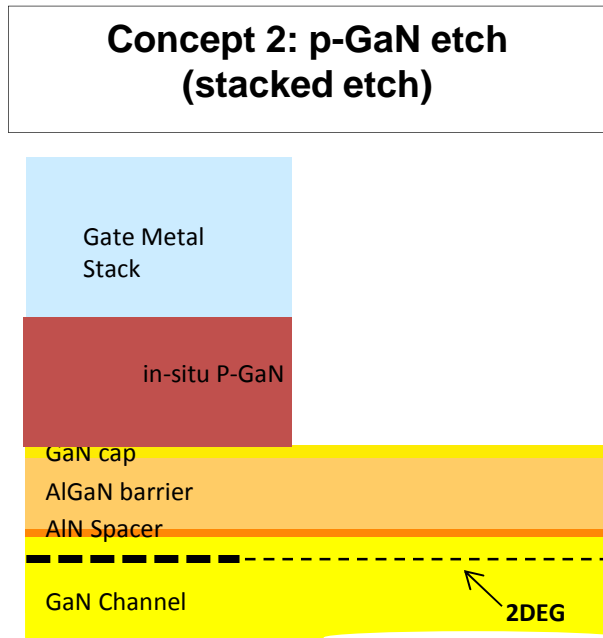
CONTROLLED BARRIER RECESS - INTEGRATED RESULTS



To be investigated:

- Effect of wet clean
- Effect of pressure in dry etch
- Effect of gas additive Cl₂, SF₆, CH₃F

CONCEPT 2: P-GaN HEMT



Principle: Mg-doped GaN locally lifts up conduction band below gate area unless $V_{th} > 0$ is applied to the gate electrode (E-mode)

Etch

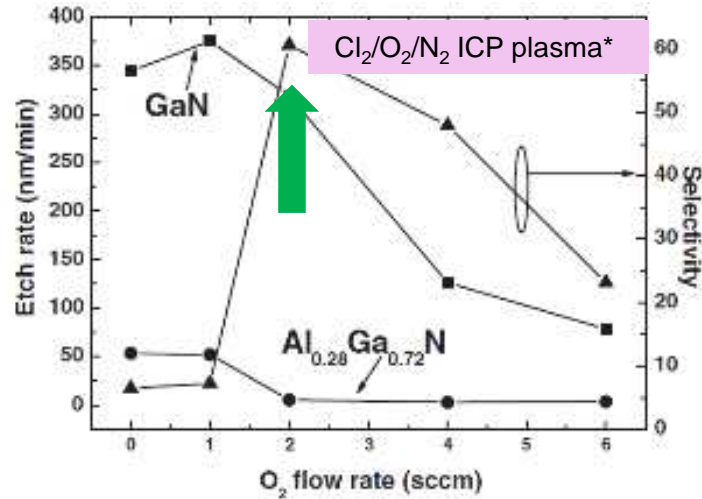
- h
 - p
 - M
 - C
 - L
-
- PR based pGaN etch
- E123200 5.0kV 2.8mm x50.0k LA100(U) 1.00um

Parameters that affect the etch result:

- presence of photoresist
- HM nature (oxide or nitride)
- % of Al in AlGaN barrier
- Chamber conditioning (CWAC)

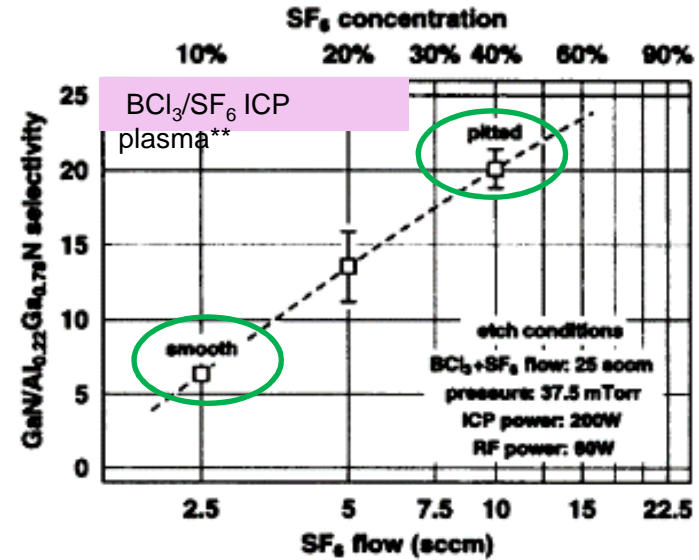
HIGHLY SELECTIVE PGaN ETCH

- LITERATURE*/**



	Cl ₂ /O ₂ /N ₂ Chemistry
Selectivity layer	Formation of Al _x O _y
Critical parameters	<ul style="list-style-type: none"> Cl₂ flow O₂ flow Pressure ICP power V_{bias}

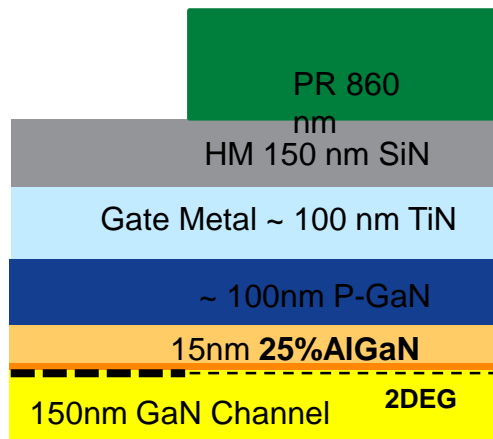
*Highly Selective Dry Etching of GaN over AlGaN Using Inductively Coupled Cl₂/N₂/O₂ Plasmas
 Jpn. J. Appl. Phys. Vol. 42 (2003) pp. L 1139–L 1141
 Part 2, No. 10A, 1 October 2003
 The Japan Society of Applied Physics



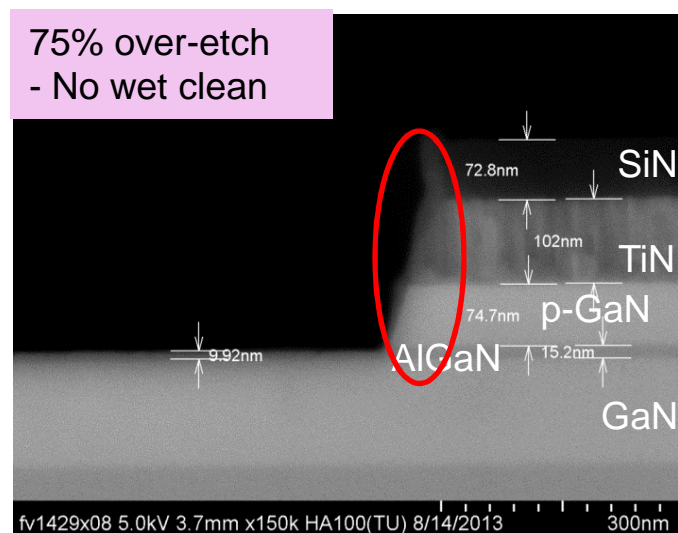
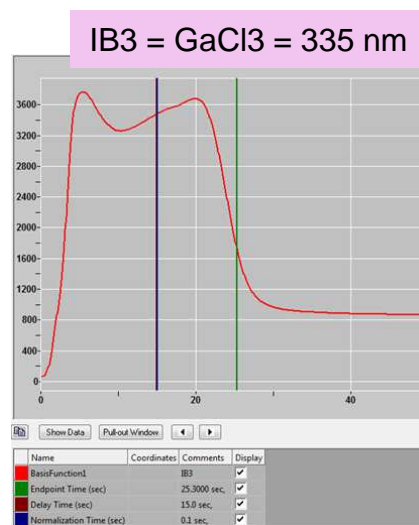
	Cl ₂ /O ₂ /N ₂ Chemistry
Selectivity layer	Formation of AlF ₃
Critical parameters	<ul style="list-style-type: none"> SF₆ flow Pressure ICP power V_{bias}

**SELECTIVE DRY ETCHING OF GaN OVER AlGaN IN BCL₃/SF₆ MIXTURES
 D. BUTTARI, A. CHINI, A. CHAKRABORTY, L. MCCARTHY, H. XING,
 T. PALACIOS, L. SHEN, S. KELLER, AND U. K. MISHRA
 Department of Electrical and Computer Engineering,
 University of California Santa Barbara, Santa Barbara, California 93106, U.S.A.

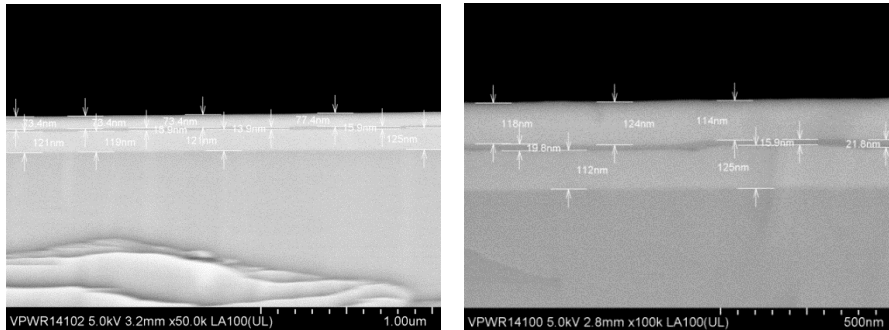
Cl₂/O₂/N₂ PLASMA - 1-STEP RESULT



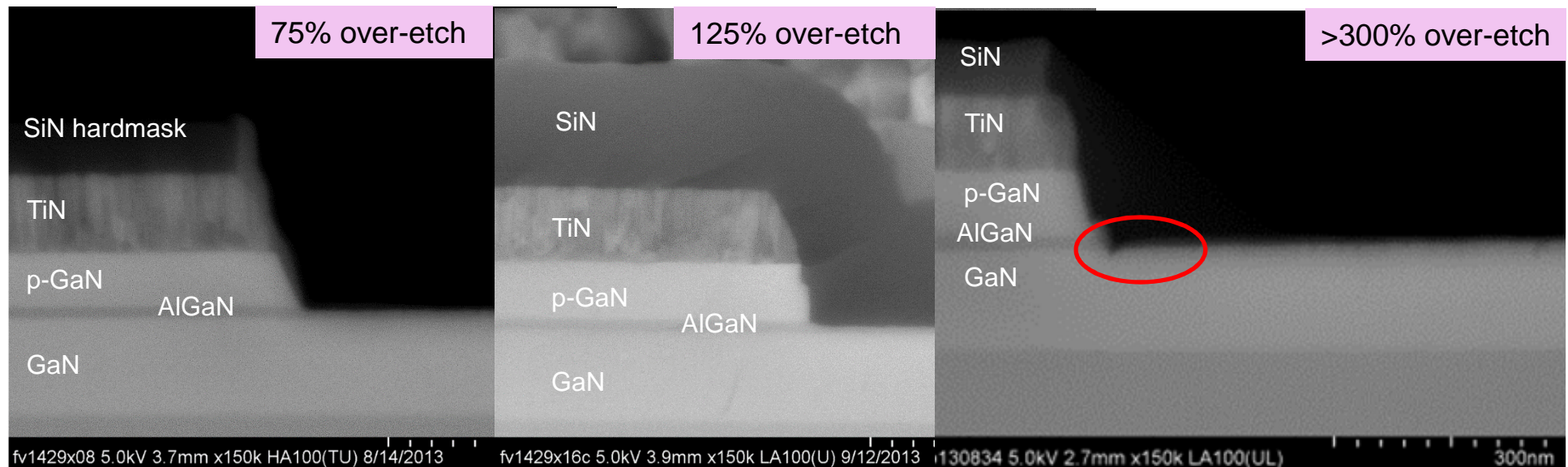
	Cl ₂ /O ₂ /N ₂ Chemistry
Tool(s)	LAM Alliance A6, TCP9600 (SiN+TiN) LAM Domino, Versys 2300 (p-GaN)
Sequence	<ol style="list-style-type: none"> Lithography SiN+TiN etch <ol style="list-style-type: none"> SiN HM etch: SF₆/O₂ TiN Etch stop on p-GaN: SF₆/O₂ Resist strip – AlGaIn covered P-GaN etch (1 step) <ol style="list-style-type: none"> Breakthrough (BCl₃/Cl₂) Selective etch (Cl₂/O₂/N₂) – on EP



Cl₂/O₂/N₂: PROCESS WINDOW - OVER ETCH VARIATION



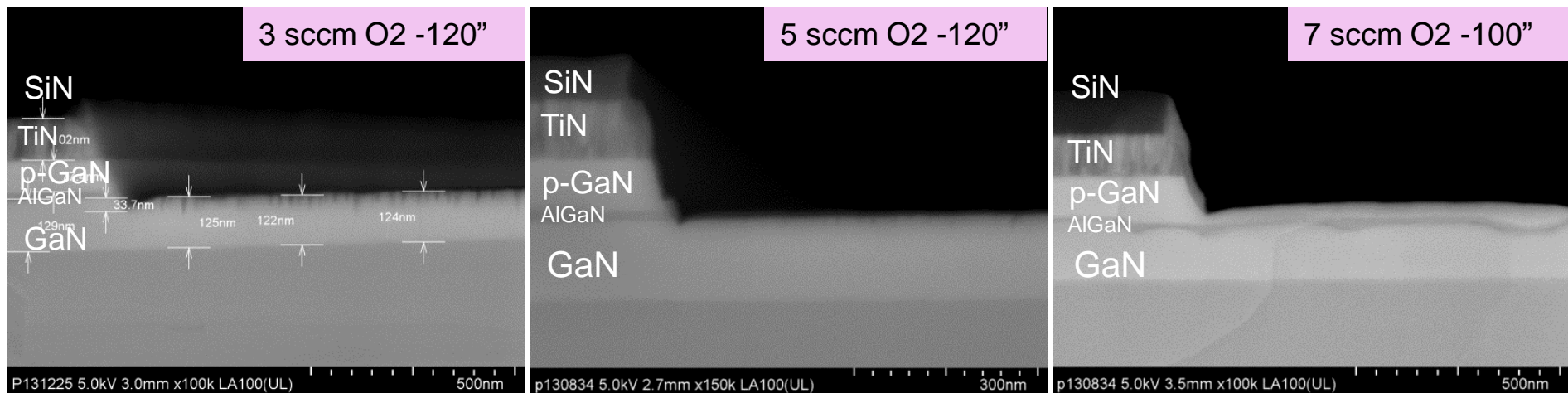
huge p-GaN thickness variation:
- 73 nm to 124 nm
→ Target 100 nm



P-GaN removed everywhere
Etch rate pGaN:AlGaN = 21:1

- Micro-trenching
- pitting

Cl₂/O₂/N₂: PROCESS WINDOW - OXYGEN FLOW VARIATION

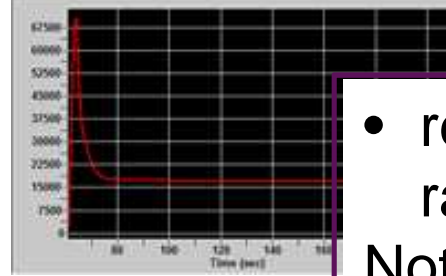
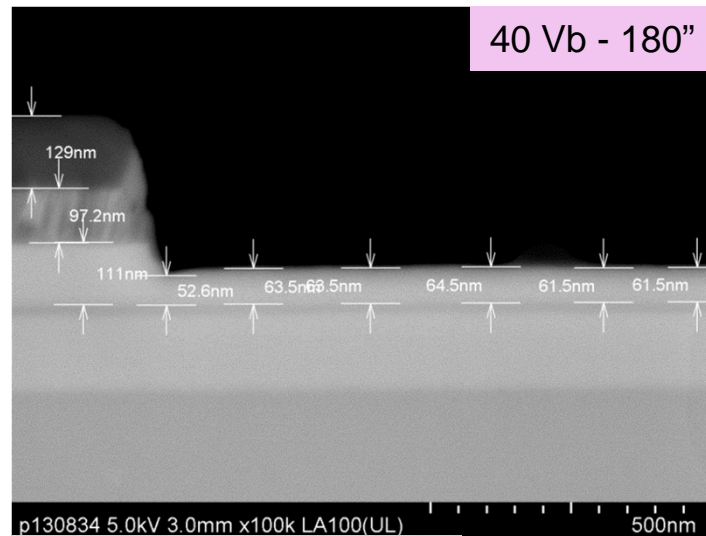
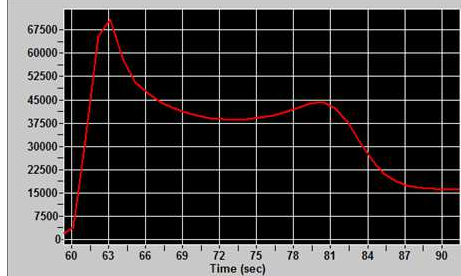
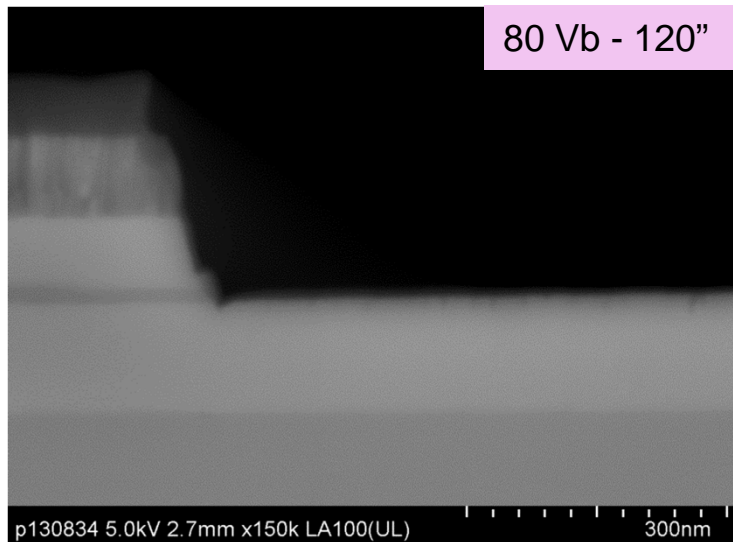


- No selectivity
- Micro-trenches/pitting

- Improved selectivity
- Some micro-trenches
- p-GaN etch rate ~ 192nm/min

- Lower p-GaN etch rate ~ 30 nm/min
- Ga-O bond formation: bond strength Ga-O >> Ga-N (etch stop !)

Cl₂/O₂/N₂: PROCESS WINDOW - BIAS VOLTAGE VARIATION



- reduced p-GaN etch rate

Not sufficient ion E to brake the Ga-O and Ga-N bond resulting in Etch stop !

Cl₂/O₂/N₂ PLASMA - MICRO-MASKING/ROUGHNESS

Our observation:

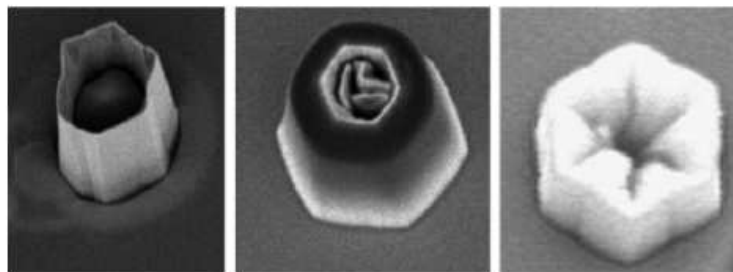
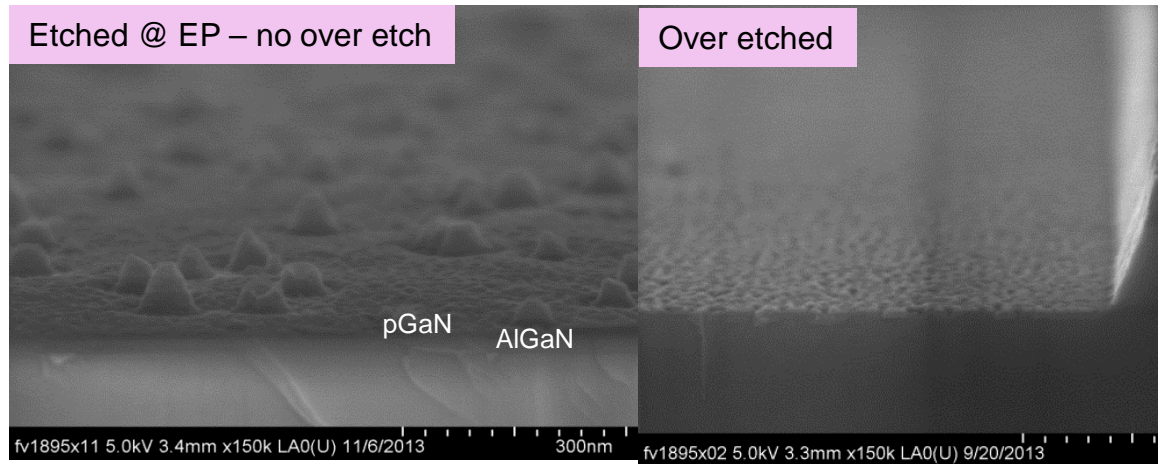


FIG. 15. SEM image columnar defects observed at the etched surface.

Mechanism*

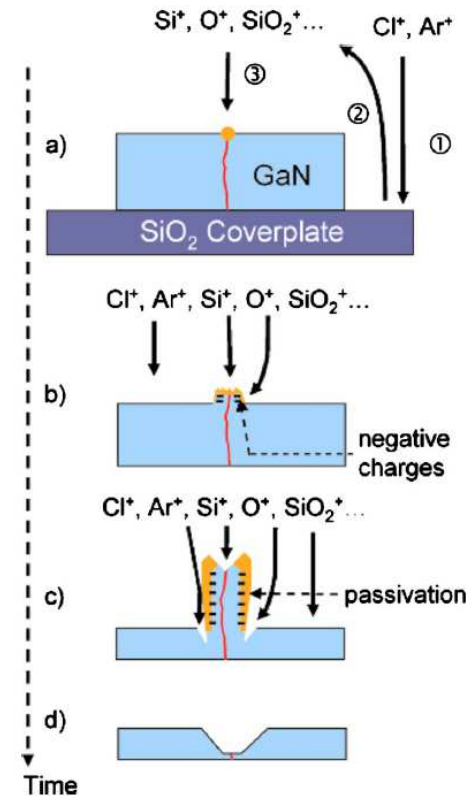


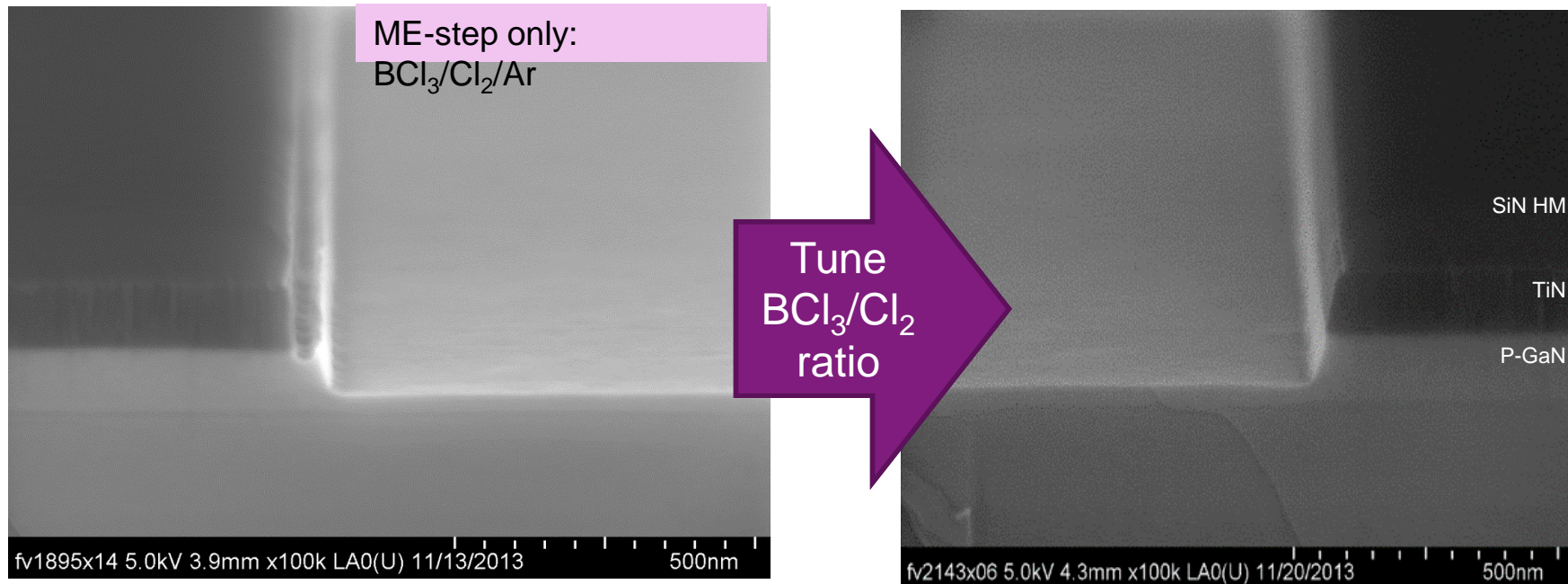
FIG. 14. (Color online) Schematic of a possible mechanism of formation of columnar defects. (a) Preferential decoration of dislocation, (b) column creation and passivation layer, (c) cavity at the top of the columnar defect and trenching at the bottom, and (d) column removed leaving a cavity.

*J. Ladroue, et al., "Deep GaN etching by ICP and induced surface defects", J. Vac. Sci. Technol. A28 (5), Sep/Oct

2010 p1226

Cl₂/O₂/N₂ PLASMA - MICRO MASKING / ROUGHNESS OPTIMIZATION

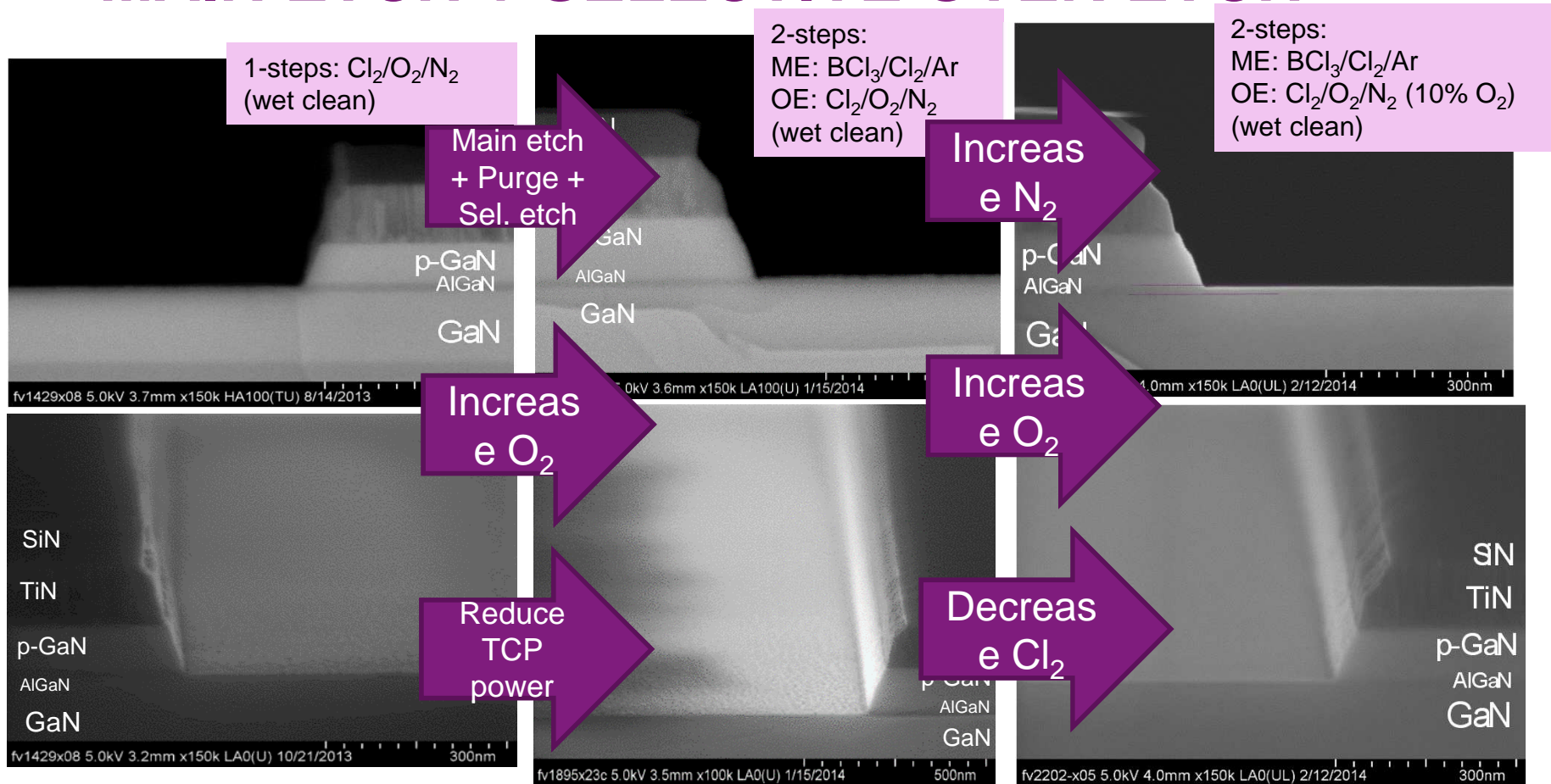
- Introduce main etch + selective over etch:
- introduce CWAC !



- Remove TiN residue's
- De-oxidize GaN

- Improved side wall protection
- avoid micro-trenching
- reduce lateral TiN attack
- Etch rate ~ 29.5 nm/min

Cl₂/O₂/N₂ PLASMA SURFACE ROUGHNESS - MAIN ETCH + SELECTIVE OVER ETCH



- Ar Purge step after main etch to remove BCl₃
→ BCl₃ reduces available oxygen

- Increase O₂ flow for improved selectivity
- Decrease Cl₂ / increase N₂ flow for improved surface morphology
- AlGaIn loss observed 2 to 4 nm

CONCLUSIONS

- ❑ 2 E-mode device concepts have been proposed
- ❑ both concepts require particular etch development:

- ALE approach: slow I_{ds} - V_{ds} Power transistor very controllable etch rate based on

alternat

- Select

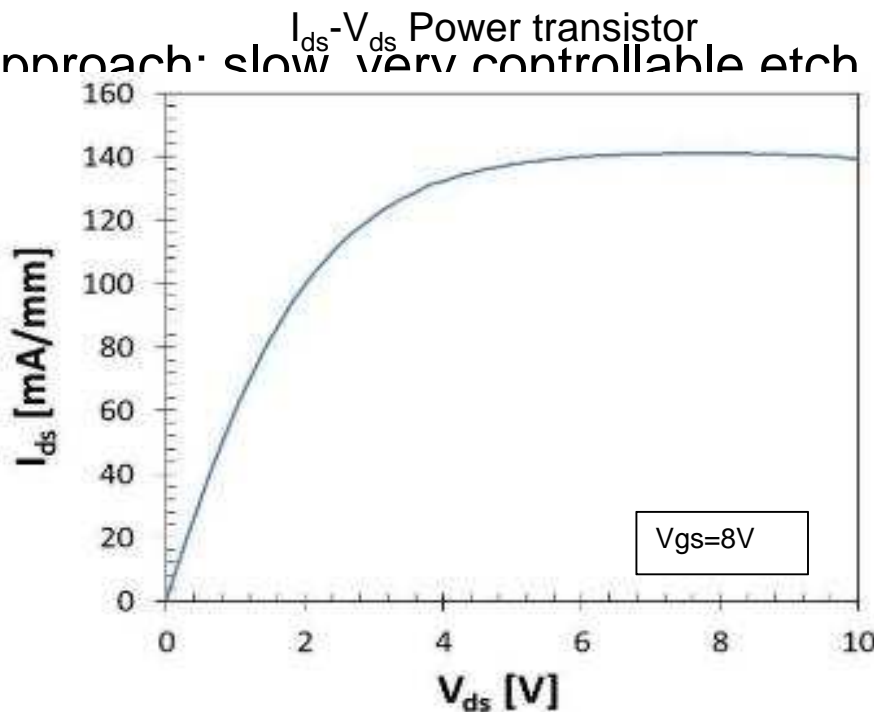
sma

AlG

sputtering

- ❑ both cc

transist



O_2 (or SF_6)

roughness

ce (effect of Si

node power



**THANKS FOR YOUR
ATTENTION !**

