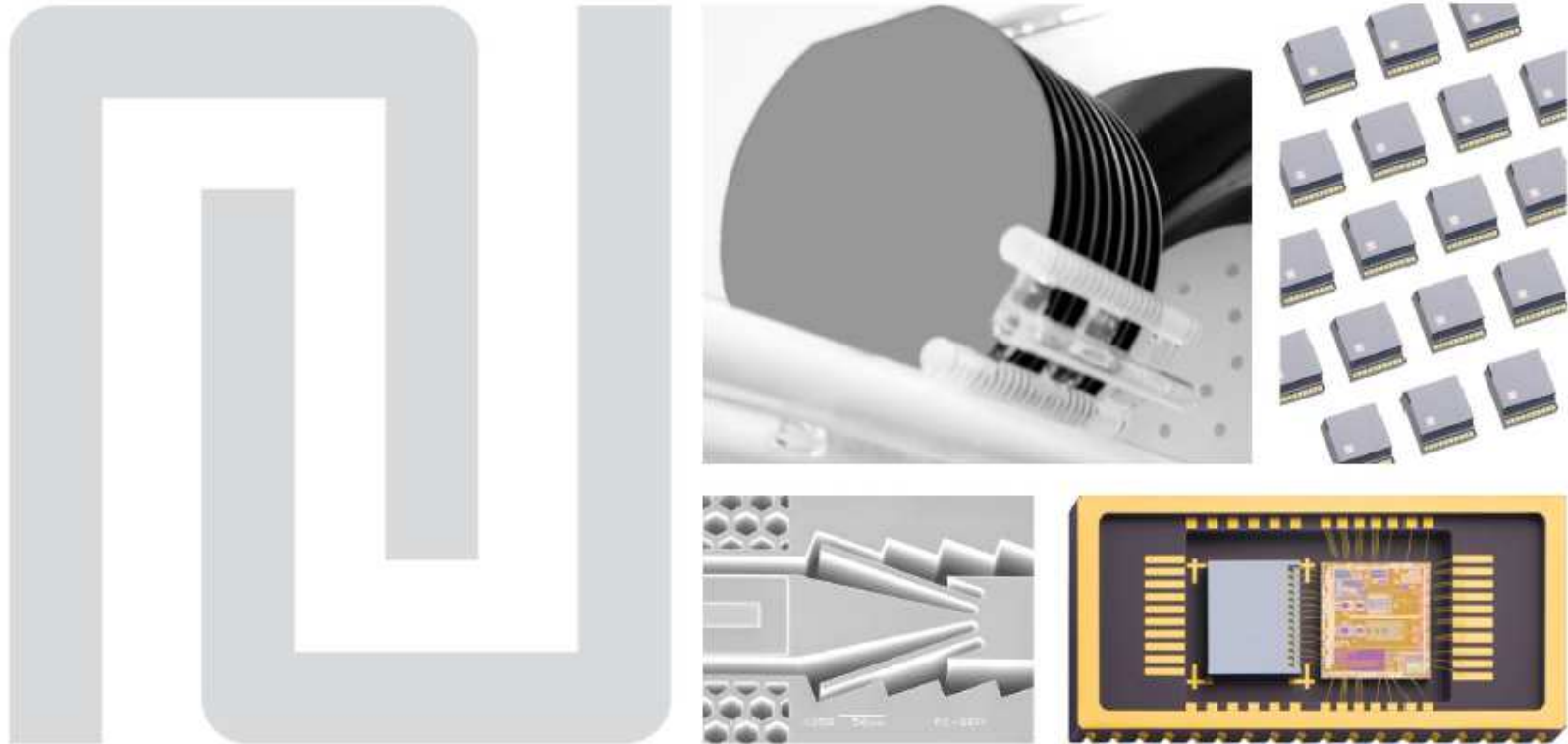


ENVISION MEMS | DELIVER MEMS



Tronics Submicron Technologies for MEMS

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tronics 

Contents

- ❑ **Tronics overview**
- ❑ **Tronics technical evolution**
- ❑ **Submicron technologies at Tronics**
- ❑ **Summary**



Tronics Overview

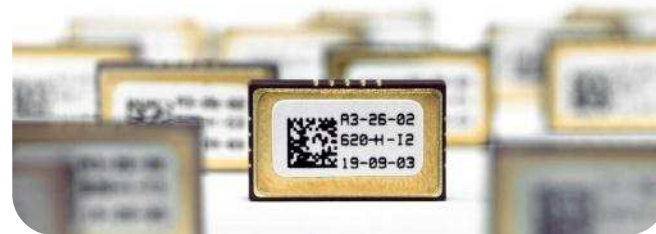
Key facts about Tronics



in the MEMS business



high-end sensors delivered



[2012] : **22 M\$, 90 employees**

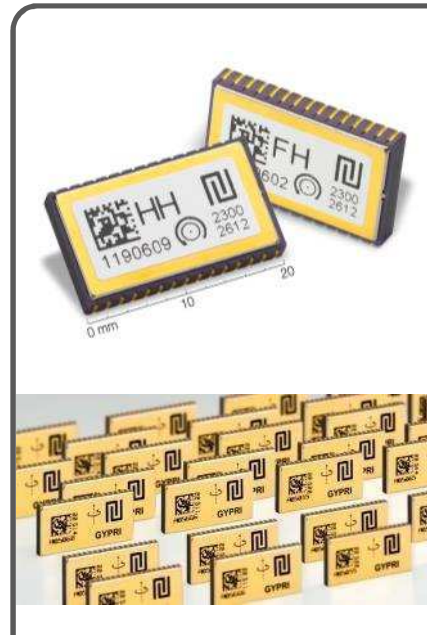
We offer solutions for...



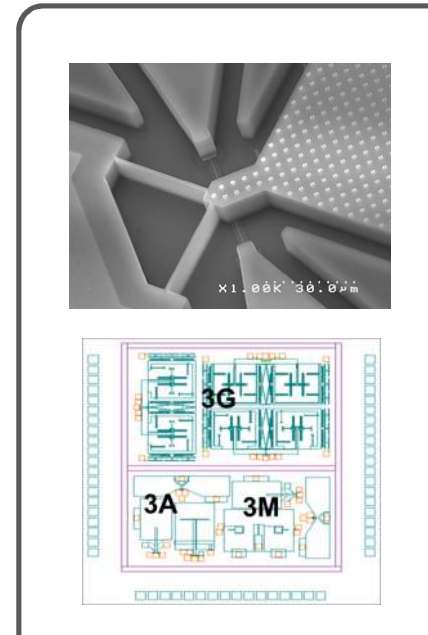
Full Service MEMS Foundry



Advanced MEMS Development



High Performance Inertial Sensors



Consumer Inertial Technologies

Flexible IP model for custom products manufacturing

Full Service MEMS Development & Manufacturing

MEMS= Micro Electro Mechanical Systems; *Mechanically active components*



Volume Manufacturing – Exotic Processes – Custom Components

Global Company | Local Support

San Francisco

Beijing

Tokyo

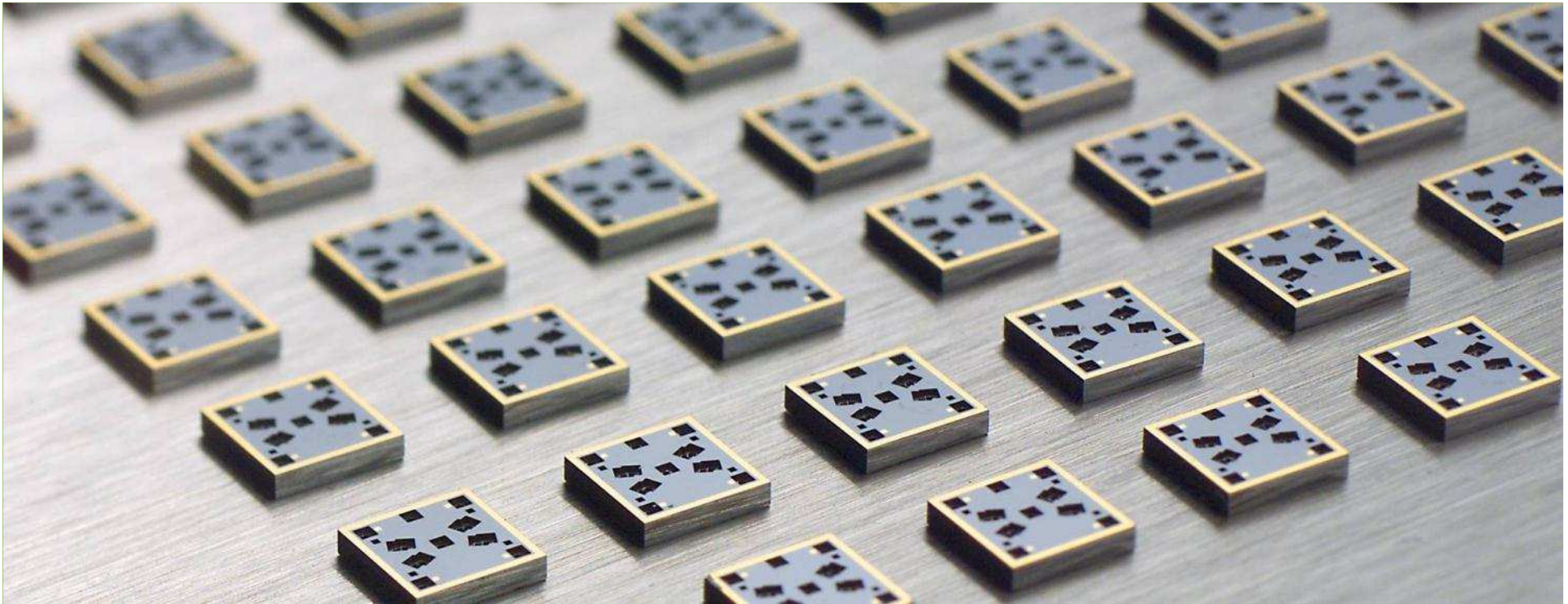
**NORTH AMERICAN FACILITY
DALLAS, TX, USA**

- 6" fab, Class 100
- 20,000ft² clean room
- 20 employees
- 50k wafers/yr

**EUROPEAN FACILITY
GRENOBLE, FRANCE**

- 6" fab, Class 10-1000
- Assembly line
- Test & calibration
- 70 employees
- 10k wafers/yr

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Tronics technical evolution

Tronics technology & product history 1/2

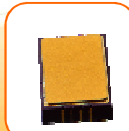
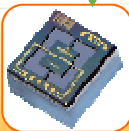
1997 1998 1999 2000 2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011 2012 2013

“Initial” technos
- bulk
- Released SOI

New Techno
- SOI/cavity
- DRIE

Vacuum
at package
level

Own fab
Crolles



Technical status
Critical dimension = 3µm

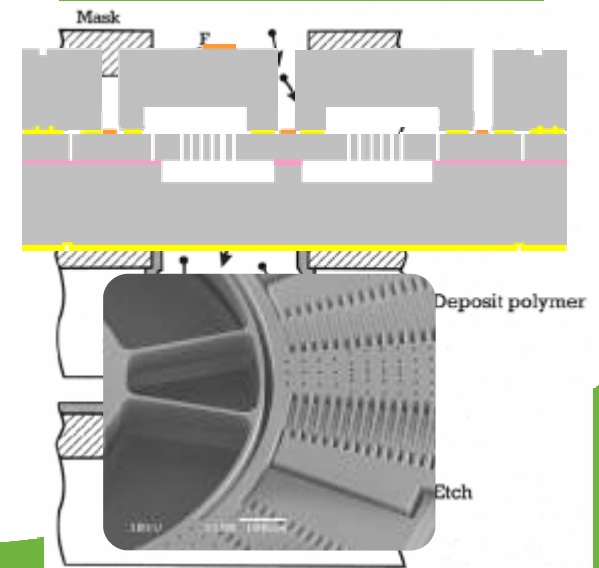
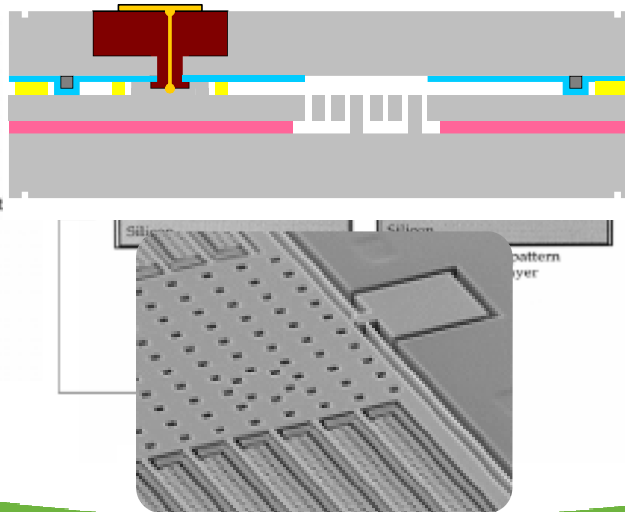
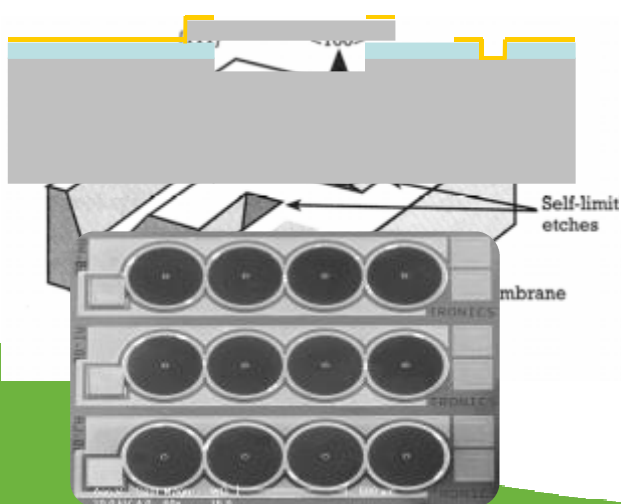
Limited by process/eqt/integration

Development & industrialization

Bulk techno
KOH/TMAH

Surface techno
Wet release/poly Si

High aspect ratio
DRIE



Which type of evolution ?



Clear target
Decrease cost/price
Increase performance/reliability



Tronics choice = Miniaturization
Continuous Improvement
Design / Process / Supply



Shrink
active part

↓ Critical Dim.

↗ SOI/PolySi
Thickness

Develop
shrink inactive part

Bonding seal
→ Metal

Interconnect
→ TSV

Optimize
supply chain

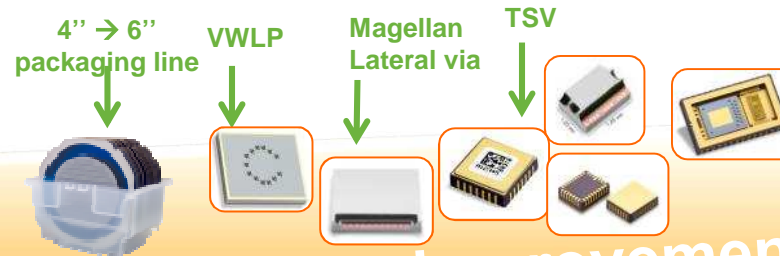
Wafer size
4" → 6"

Supress package
→ VWLP

Tronics technology & product history 2/2

1997 1998 1999 2000 2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011 2012 2013

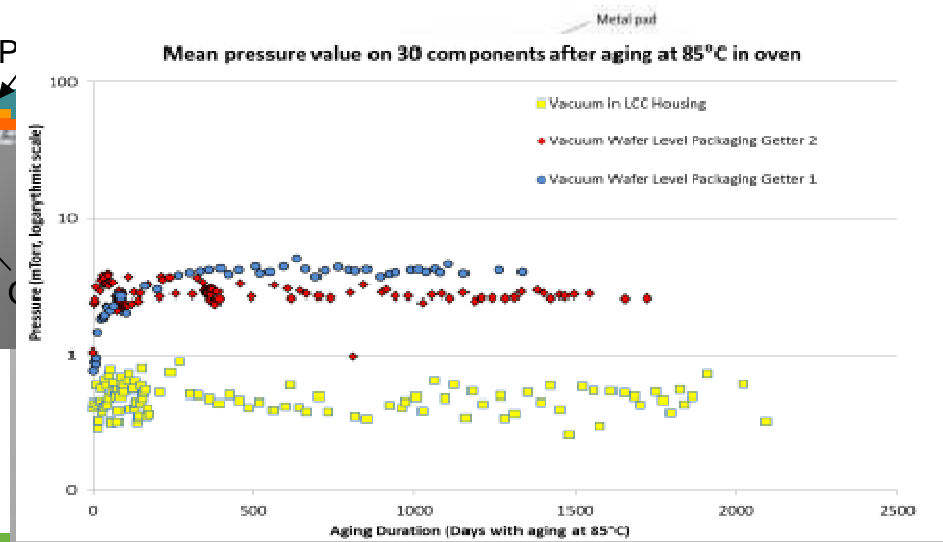
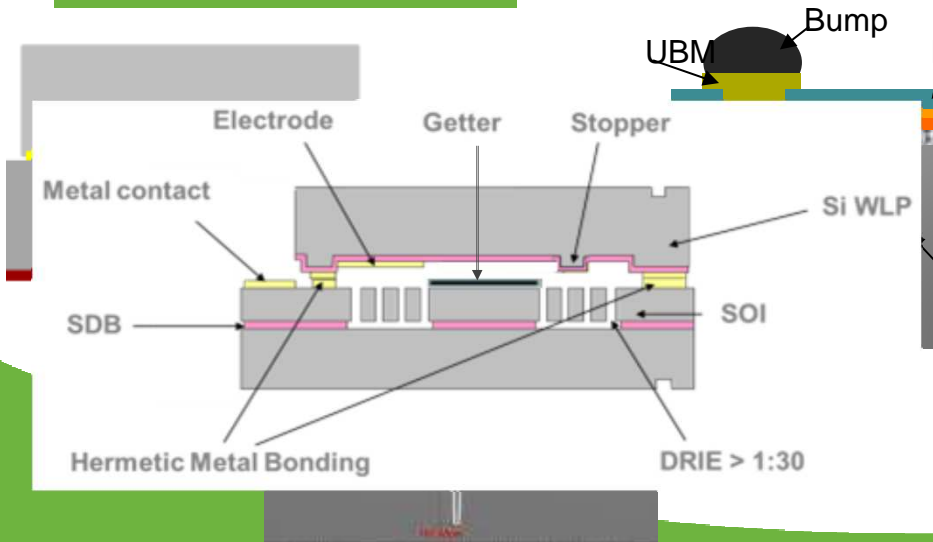
Technical status
Critical dimension = 1,5 μm
 Divided by 2 compared to first technologic roadmap



Continuous improvement

Increase Proof mass thickness \rightarrow SV last able to decrease the gap CD to 1,5 μm Cu TSV

VWLP
 Aging & characterization



150 μm

Then, Same target, Same evolution ?

Re-Shrink active part

CD limited by capacitive principle

Need minimum mass for performances



Develop shrink inactive part

Sealing - Need min width for hermeticity

TSV optimization → limited gain



Optimize Supply chain

Wafer size 6" → 8" → Need high volume → Expensive

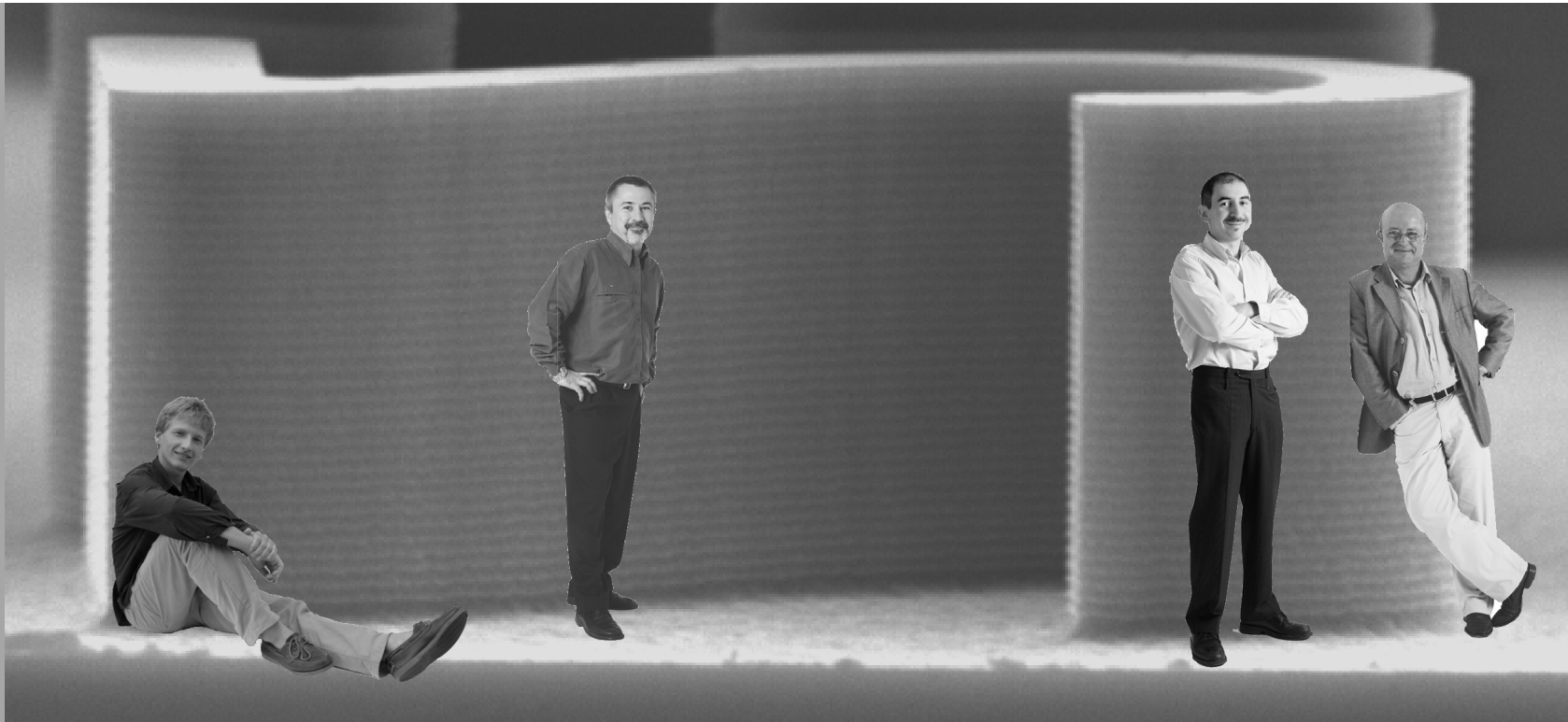
VWLP done → Limited gain



Tronics fact

We can't continue in the same way !

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Tronics technologic roadmap

Standard microtechnology

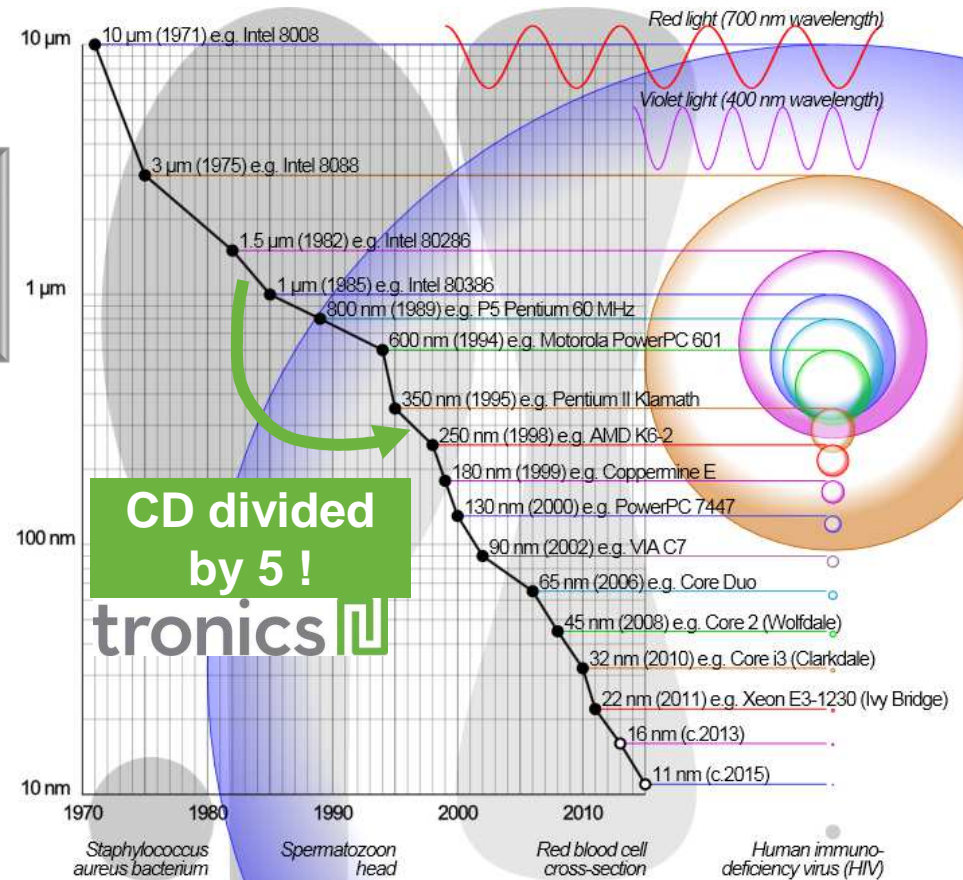


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Submicron for MEMS & Tronics

Submicron exist since long time in Microelectronic
 Continue evolution of tools & know how (Moore law)
 → Technical solution are here !

Critical dimension targeted =
0,3µm



For Tronics : 'REVOLUTION' rather than EVOLUTION !



Submicron in MEMS – What do we need ?

1st decision for this CD evolution → Equipment invest



Lithography equipment

Stepper CD=0,3 μ m



Nano-imprint CD=0,1 μ m



Dry etch equipment

DRIE etcher



Control equipment

High perf. SEM



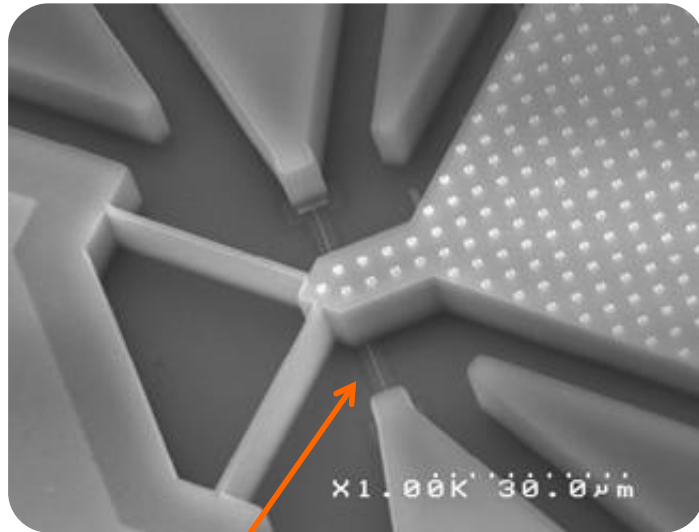
Submicron Technologies

2nd decision for this CD evolution → Technology invest

M&NEMS

Breakthrough submicron technology

leti → trionics



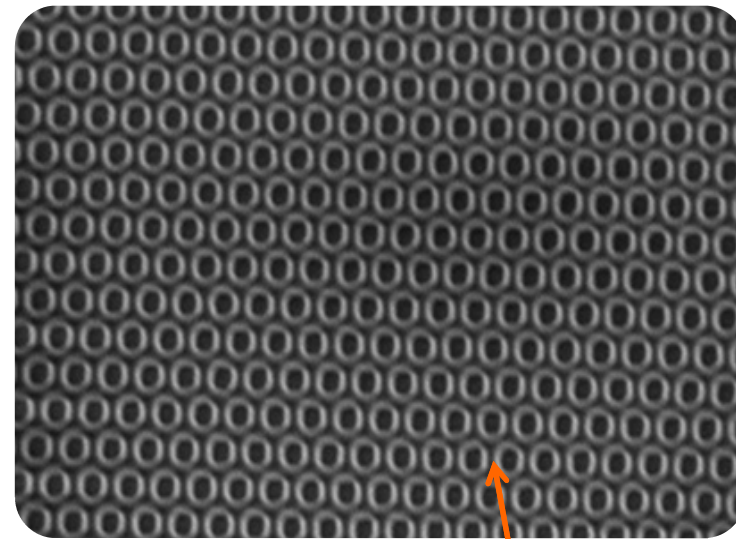
Si Nanowire

Critical Dimension = $0,5 \mu m$

NIL

Industrialized submicron technology

trionics



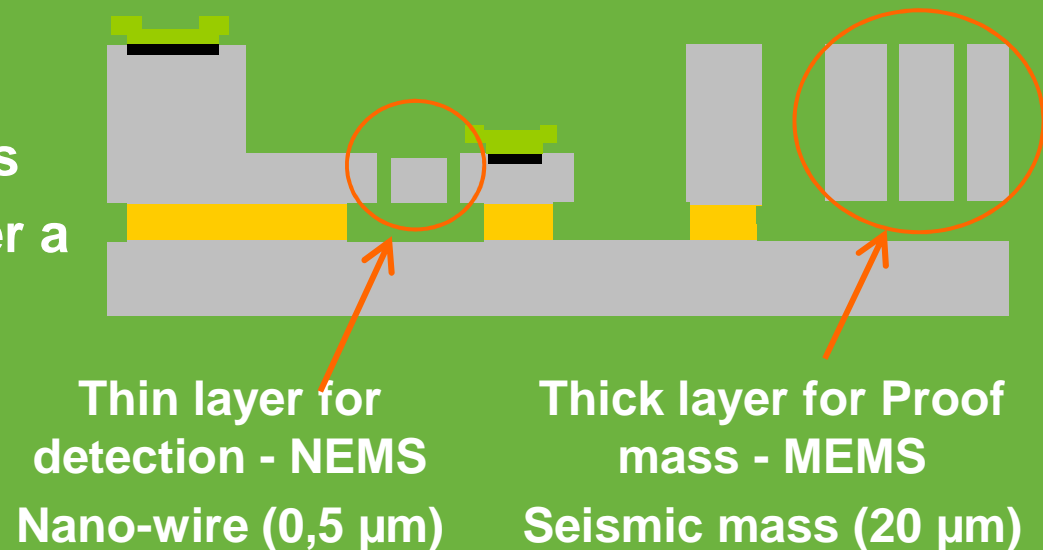
Submicron holes over large surface

Critical Dimension = $0,3 \mu m$

Submicron technology : M&NEMS

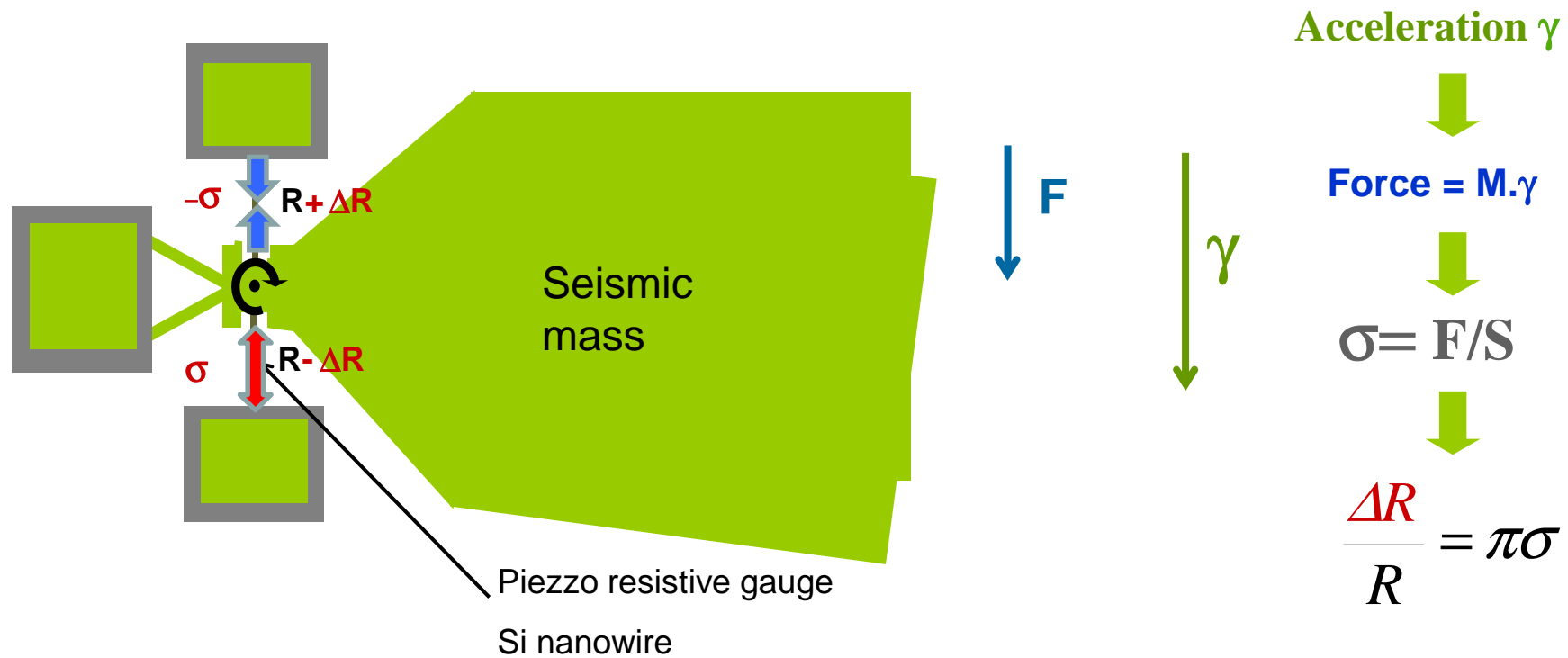
New disruptive technology

- 2 hugely different thicknesses
- Nanogauge permits to recover a large part of the force (no dilution in the thickness)



**Tronics objective :
Development**

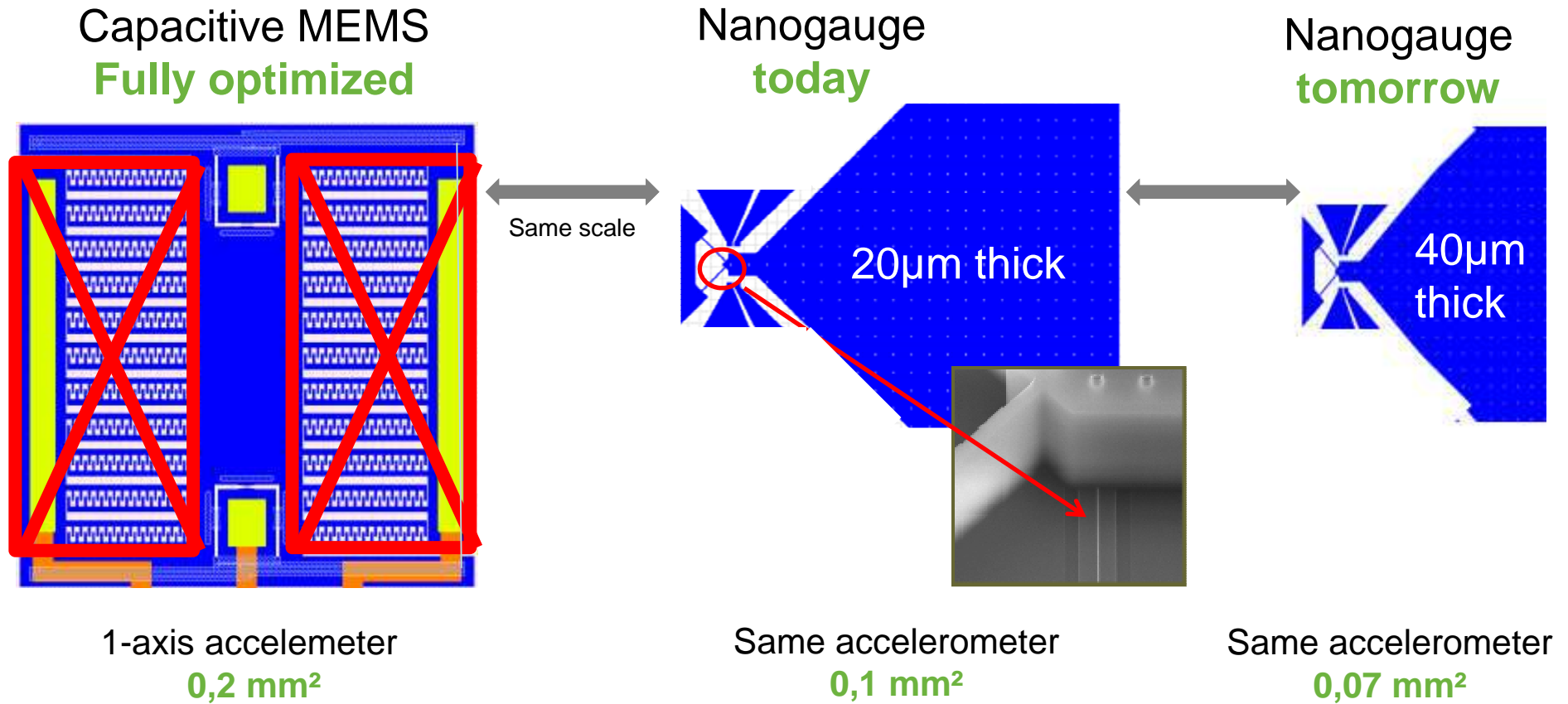
Piezzo Resistive Effect: Working Principle



Gauges made by monocrystalline Silicon Nano-wire
No gauge bending, only compression or strain

Standard piezzo-resistive detection → Standard ASIC

Roadmap to extreme miniaturization



M&NEMS technology decrease critical dimension
but also die size and finally cost

M&NEMS Process

Cavity



Seals



M&Nems Patterning



Cap seal



+



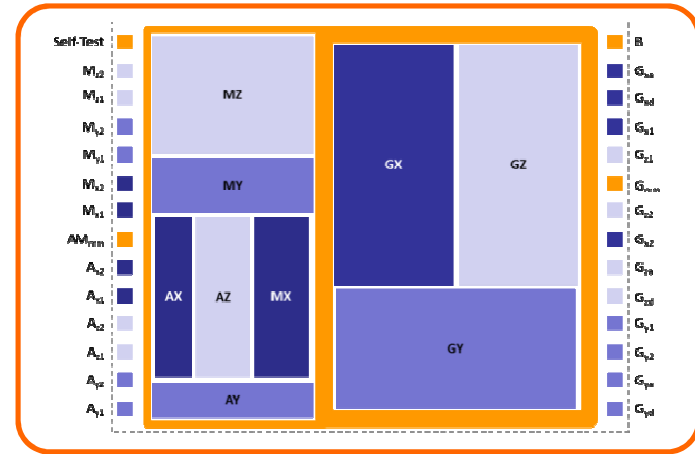
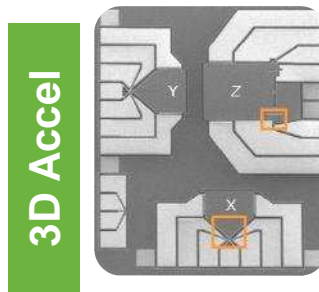
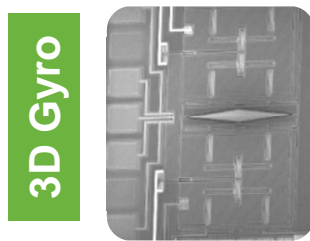
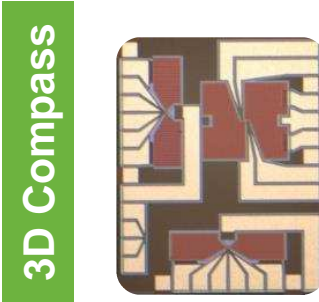
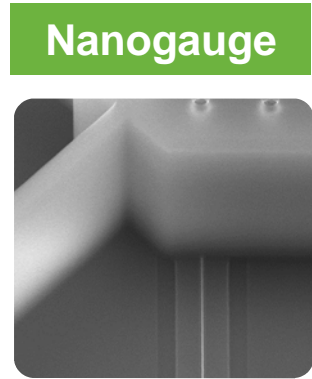
Via opening



Thinning



M&NEMS Application



1 single technology
9 DOF in a single chip

➔ Compared to standard MEMS technology, Area gain x4

Motion sensing for mobile applications

Application targeted : consumer market



6 DOF for Gaming
(3D Acc. + 3D Gyros)

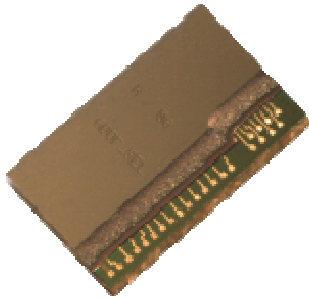
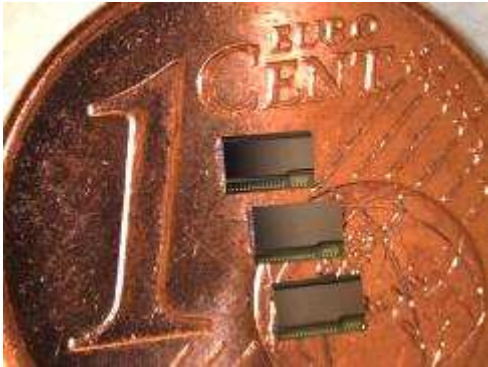


6 DOF for Augmented reality
(3D Acc + 3D Compass)



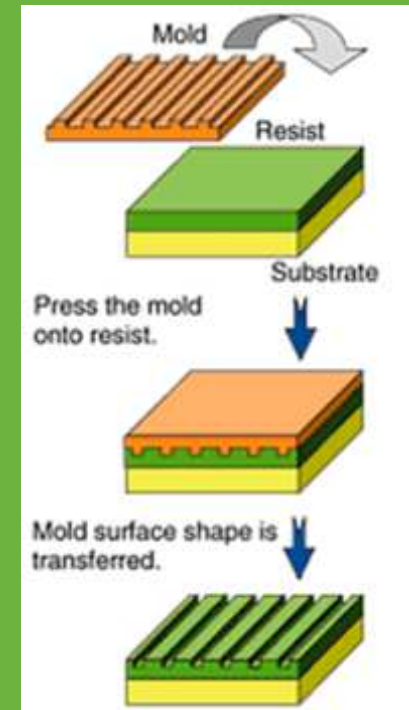
9 DOF for Indoor location & Pedestrian Navigation
(3D Acc. + 3D Gyros + 3D Compass)

February 2014 : 1st M&NEMS prototype - 6 DOF (3A3G)



Submicron technology : NIL

« Old » technology mainly used in university
Well adapted for glass processing
Critical dimension ~ 10 nm



Tronics objective :
Industrialization

NIL vs stepper lithography

Tronics criteria	NIL	Litho i-line	Litho DUV
Capability dimensions - Squareness - 0.2 μm spacing	++ Can handle dimensions down to 10nm	-- 0.28 μm bottom limit. 'squareness' <u>not possible</u>	+ Spacing is feasible, but 'squareness' difficult to obtain
Timing required to setup technology	+ Tool can be easily implemented	-- Not an option	-- Requires >1yr development
Maturity technology	-- NIL not used in production	++ HVM technology	++ HVM technology
Process complexity	+ Requires separate stamp manufacturing	- Coating-litho Few restrictions on environment/timing	-- Coating-litho Resist sensitive to environment/timing
Pricing tool	++ ~ 300 k€	- ~ 1 M€	-- 3 M€
Pricing master/reticle	- ~ 150 k€ for 6" master need to find alternatives	- ~25 k€ phase shift mask with advanced OPC's	- ~25 k€ phase shift mask with advanced OPC's

DUV : too expensive/complicated to put in place
 i-line : impossible to pattern square structures
NIL – Best solution for required application

NIL (SCIL) process



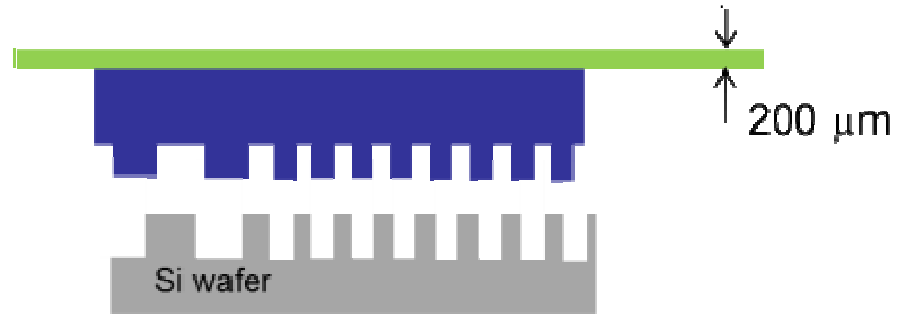
Master fabrication

Si wafer with desired pattern by e-beam



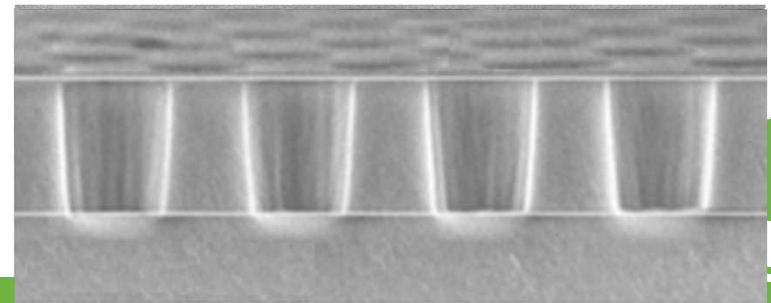
Stamp fabrication (mold)

Master replicated with polymer material on a glass frame



Imprint & etch process

- Apply hard mask & nano-imprint resist on 'stamp' in NIL resist (currently still liquid)
- UV cure → fix structures in the resist
- Stamp release
- Breakthrough etch (NIL resist residue)
- Hard mask etch
- Substrate etch
- Strip/clean



NIL technical challenges

Resist

Sol-gel resist characteristic :

- Very low viscosity (almost like water), fills easily the stamp
- SiO₂-like material, very thin layer of resist
- Stability of sol-gel resist after coating

Master

Availability of reliable source for masters paramount : University, lab, Some specialized companies (AMO, NILT)

Suppliers limited by wafersize : 6" wafer processing requires 8" master

Mostly e-beam technology → very expensive (~200k€)

Nil

Stamp release difficult

'tearing off' sol-gel resist during stamp release

Due to insufficient coverage, area defect is significantly enlarged

~ t+100s



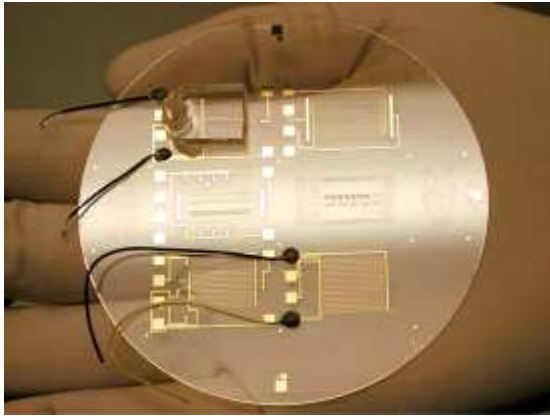
18kV X4,500 5µm TRONICS

200nm



NIL application targeted

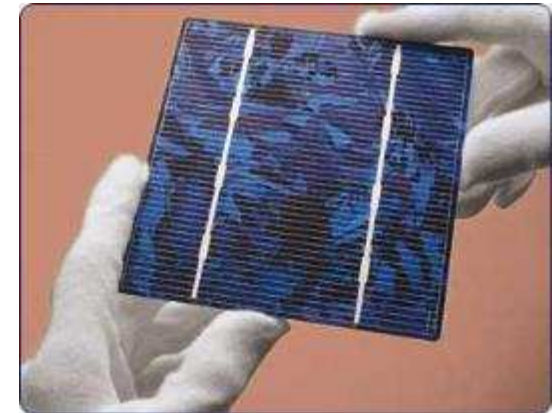
NIL for Microfluidic



NIL for Photonic



NIL for Solar



Currently in production at Tronics since end of 2012
for a confidential application

Next steps (ongoing)

Photolithography

- Resolution
(Stepper Sub- μ , Nano-Imprint)
- 3D (dry film, Spray,...)
- Lift Off

Etch

- High factor form, homogeneity
- Thickness, roughness, angle
- Material : Glass, other

Deposit

- Cu, Au Electroplating..
- Thin film magnet, W strain alloy
- BCB, SOL GEL, Piezzo...

Substrate

- Thin/Thick SOI
- Thickness: very thin to very thick
- Temporary bonding
- Glass

Back-End

- TSV, BUMPS
- Getter
- Interposer

Packaging

- Low stress
- Low price



Many development are linked to submicron



Summary

Summary

- ❑ After following the **general trend in MEMS** global evolution since 10 years
- ❑ Tronics has decided to continue to **innovate** by using emergent processes and technology directly from research.
- ❑ Since 2 years, Tronics has invested in 2 main disruptive technology :
M&NEMS & NIL.
- ❑ Tronics has entered into submicron world by jumping directly from
1,5 μ m to 0,3 μ m.
- ❑ This **internal revolution** is now a standard at Tronics and industrial product are currently delivered to customer !



Thank you for your attention !

Any « submicron » question ?