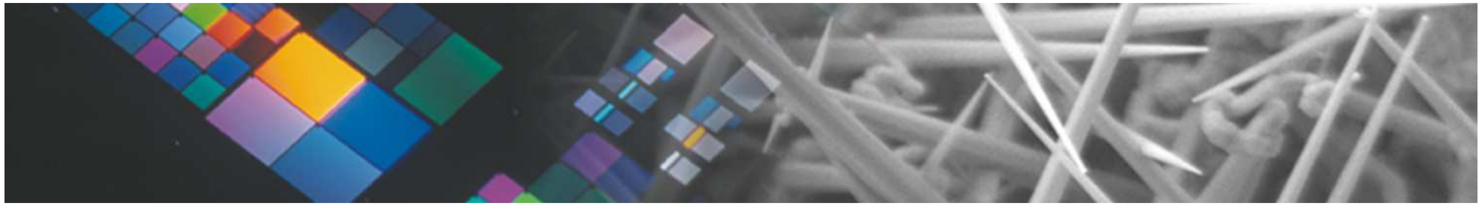


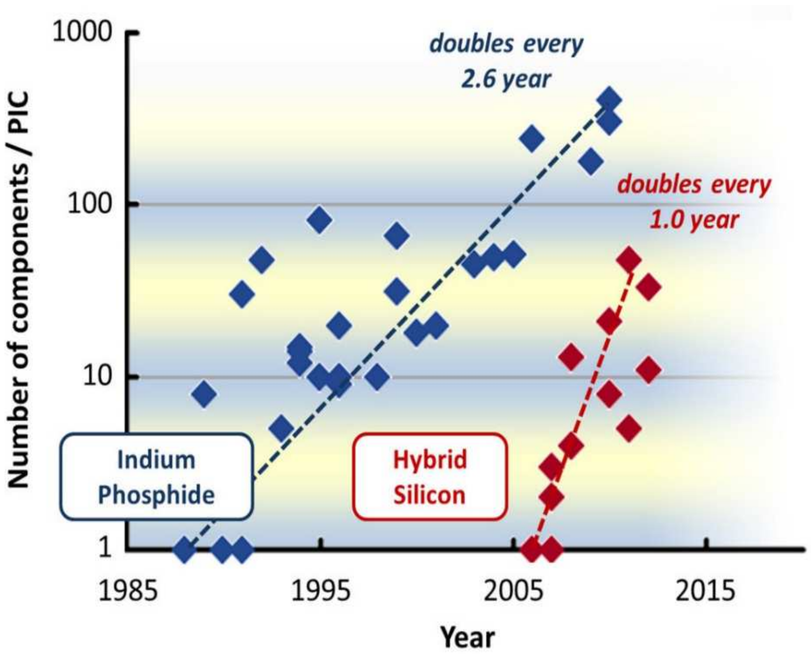
Reactor wall plasma cleaning processes after InP etching in $Cl_2/CH_4/Ar$ ICP discharge

R. Chanson[a], E. Pargon[a], M. Darnon[a], C. Petit Etienne[a], S. David[a], M. Fouchier[a], B. Glueck[b], P. Brianceau[b], S. Barnola[b]

[a] Univ. Grenoble Alpes, CNRS, LTM, CEA-Leti

[b] CEA/LETI

Hybrid photonic integrated circuit (PIC)



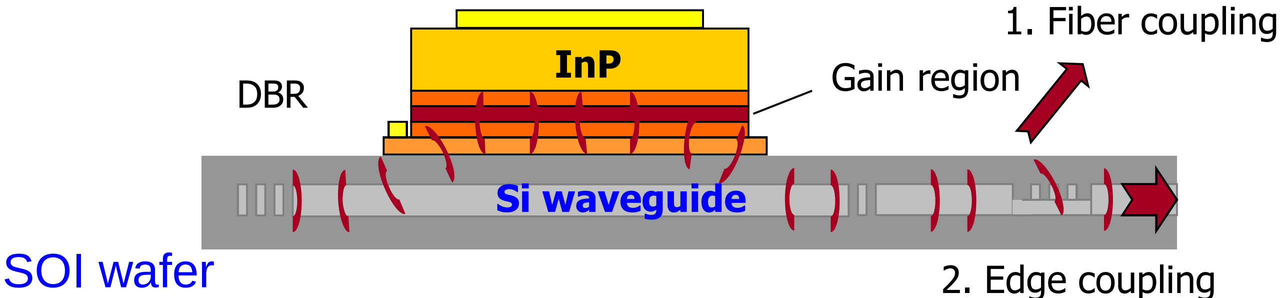
Martijn J. R. Heck, SPIE Newsroom 2013

- ❑ Photonic integration is the key to reduce size, increase functionality and reduce cost of photonic devices

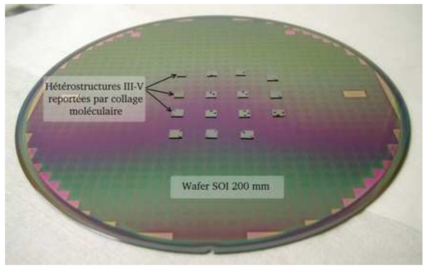
- ❑ Hybrid silicon integration combines:

- Silicon and derived components to elaborate waveguides, filter or photodetector
- III-V materials for light emitter

III-V Laser source

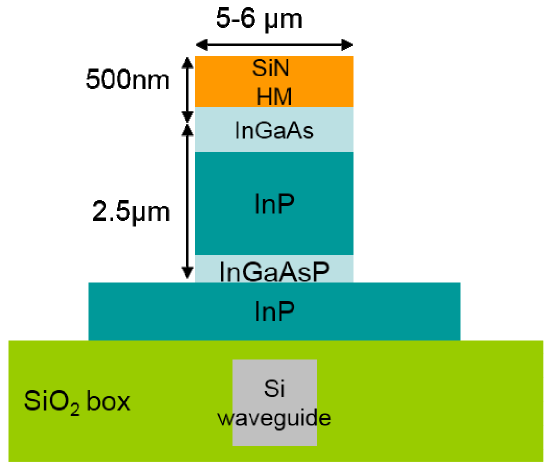


III-V integrated by molecular wafer bonding



Plasma etching of III-V materials

- Process requirements:
  1. High etch rates
  2. Anisotropic sidewalls
  3. Selectivity III-V vs SiN hard mask and SiO_2 box
  4. Minimized surface and sidewalls roughness
  5. Compatible with CMOS technology (contamination)



- Inspection of boiling points for chemistry suitability:

http://www.webelements.com

III-V	Chloride	Fluoride	Hydride
Ga	Ga_2Cl_6, 201°C	GaF_3, 950°C	$[GaH_3]_2$, 0°C
In	$InCl_3$, 583°C	InF_3, >1200°C	InH, N/A
P	PCl_3, 76°C	PF_3, -102°C	PH_3, -88°C
As	$AsCl_3$, 130°C	AsF_3, 63°C	AsH_3, -63°C

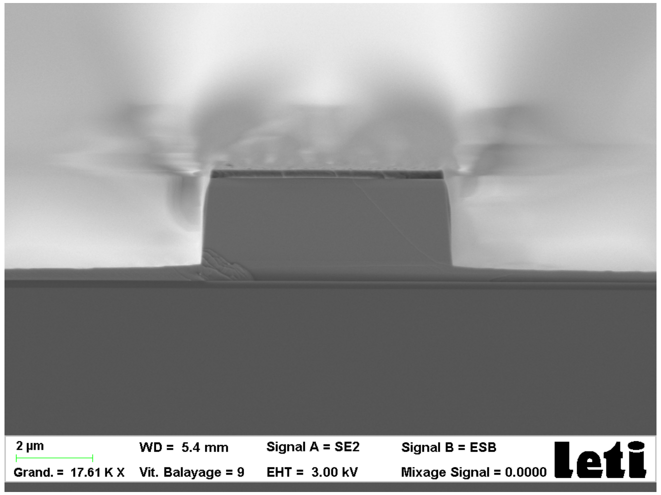
→ Ar/ Cl_2/CH_4@170°C

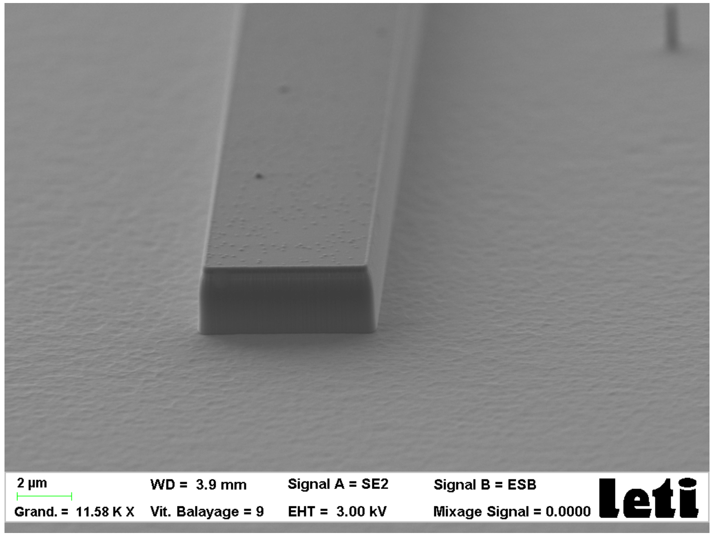
- Cl_2 ↓ Reactive etchant
- CH_4 ↓ Passivative species

- F unreactive with group III
- Cl chemistry suitable for GaAsP system
- Low volatility of $InCl_x$ compounds

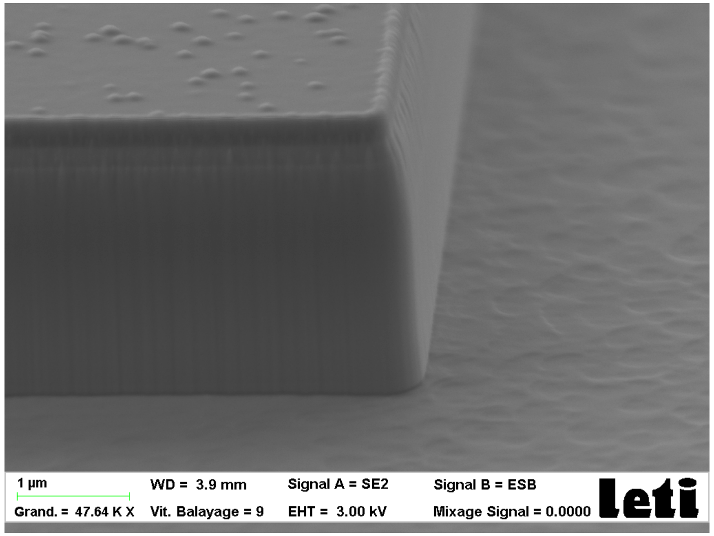
III-V plasma patterning results

Ar/ Cl2/CH4@170°C in ICP (AP from AMAT)



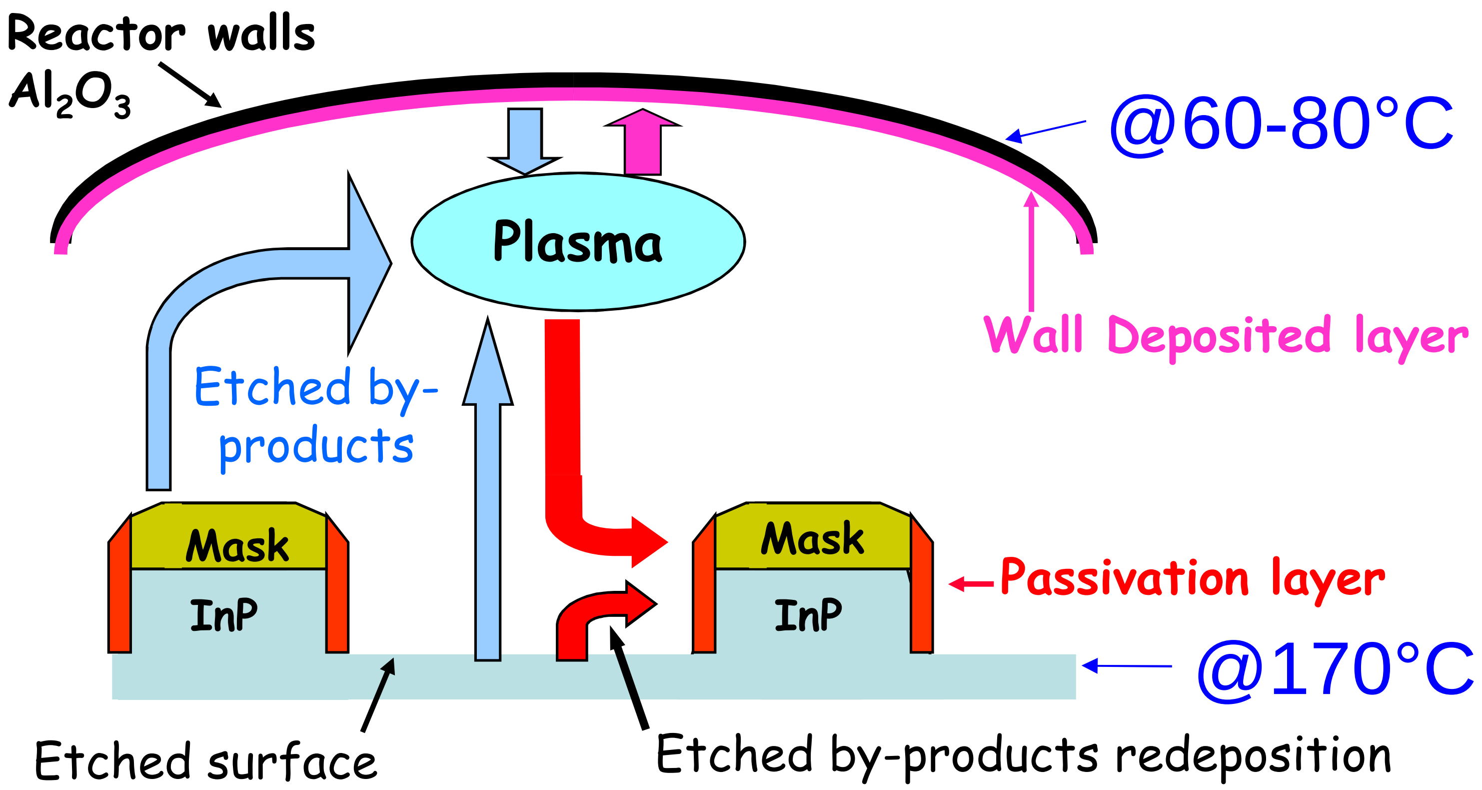


- Etch rates acceptable: 472nm/min
- III/V SiN selectivity: 14
- Anisotropy : 86°
- Surface and sidewalls roughness OK



Courtesy of P. Brianceau, CEA/LETI

Reactor wall contamination during plasma etching



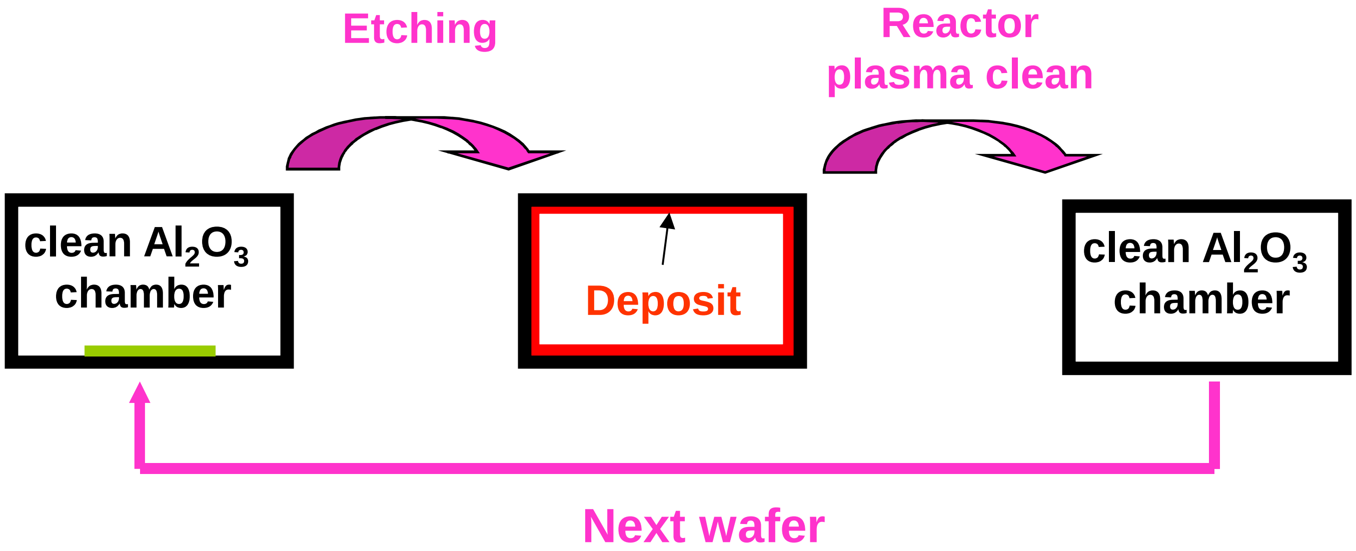
❑ Formation of coatings on Al_2O_3 chamber walls changes the plasma chemistry

⇨Causes process drift, wafer to wafer irreproducibility

Today’s strategy for process reproducibility

Changes in reactor walls conditions = process drifts

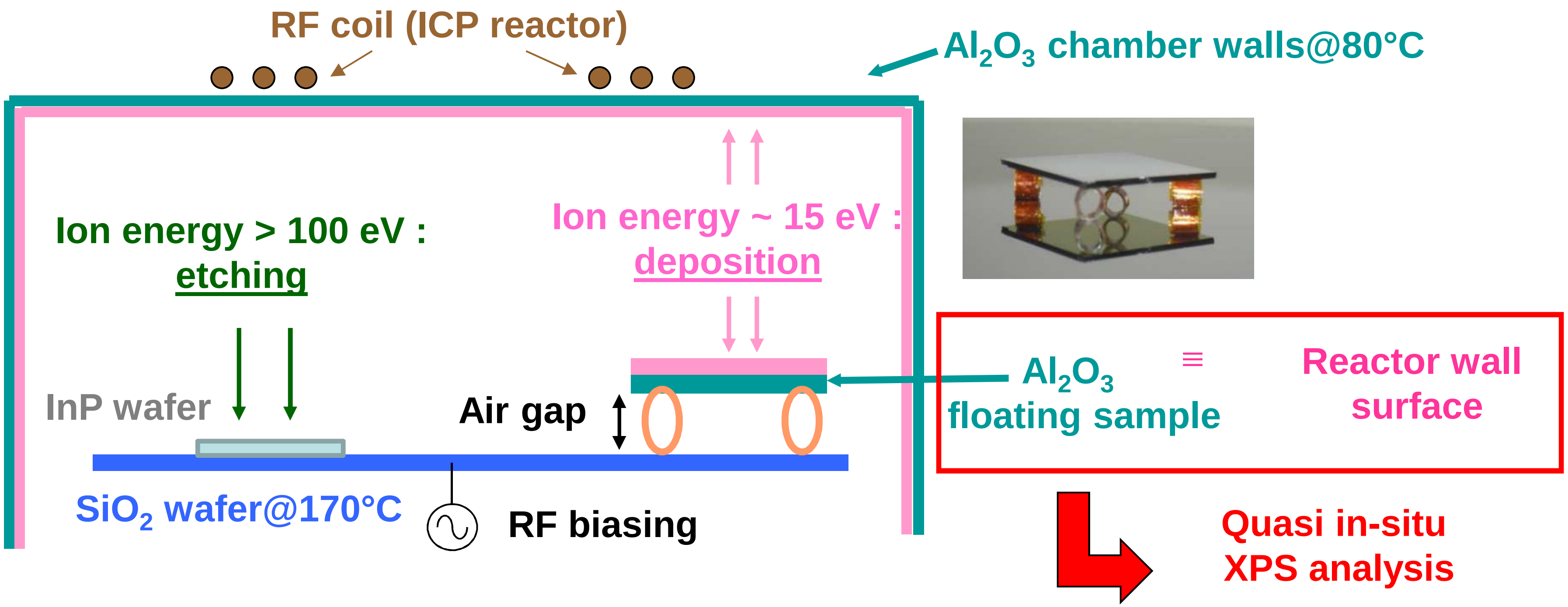
Today's strategy to get a reproducible process: *Clean the reactor between wafers*



- Aim of this study
  - ✓ Characterize the deposits formed on the reactor wall
  - ✓ Propose plasma cleaning strategies

Analyses of chamber walls coatings

"Floating sample technique": An electrically floating Al_2O_3 sample is used to simulate the reactor wall conditions

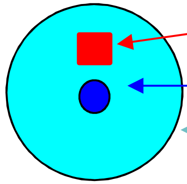


*O. Joubert, J. Vac. Sci. Technol. A **22**, 553 2004.*

Chemical nature and thickness of the **chamber wall coatings**

N.B. Use of temperature stick to monitor floating sample temperature

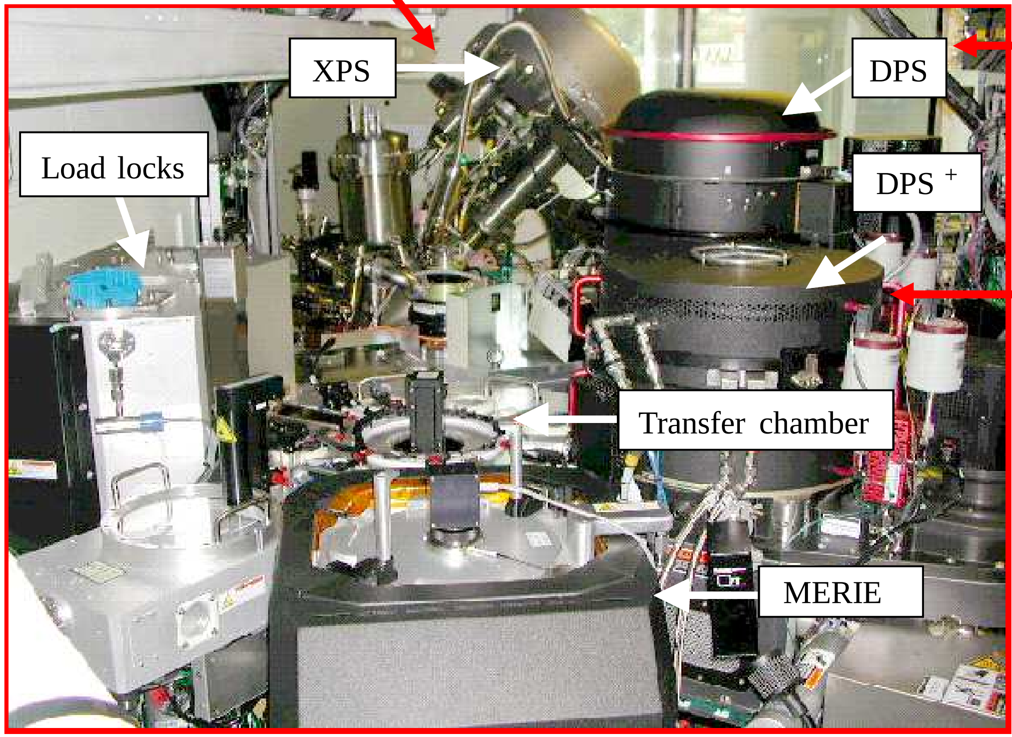
Experimental set-up



- Substrates: 2 ” InP wafer on a 200mm diameter SiO2 carrier wafer

- Etching and characterization experiments: 200 mm plasma etching plateform from AMAT

XPS: quasi in situ characterization of the coating deposit and its plasma cleaning



ICP with ESC @ 50°C
→ Reactor wall cleaning experiment

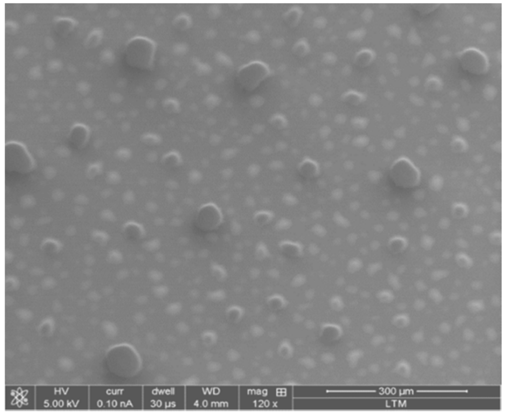
ICP with hot cathod @ 170°C
→InP etching

Characterization of the deposit on the reactor wall

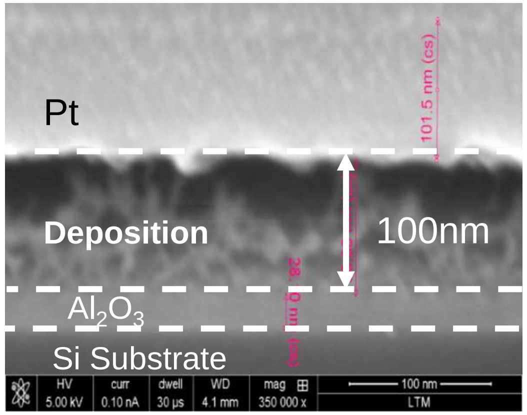
FIB-SEM
Morphological analyses of the deposit

- Deposit thickness ranging from 50 to 100nm
- Inhomogeneous rough surface

Top view

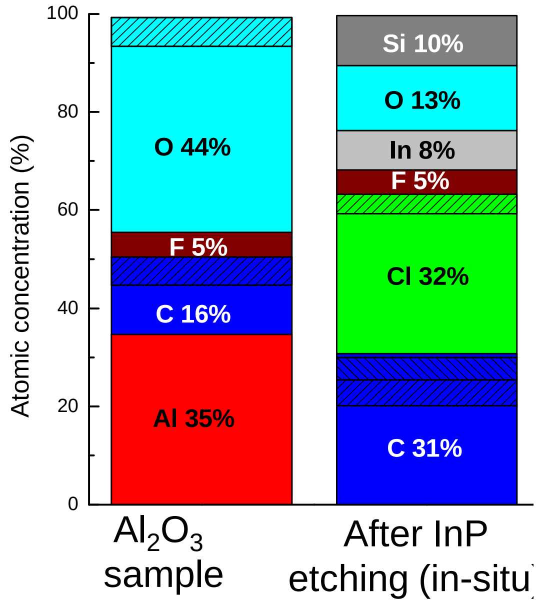


Cross section



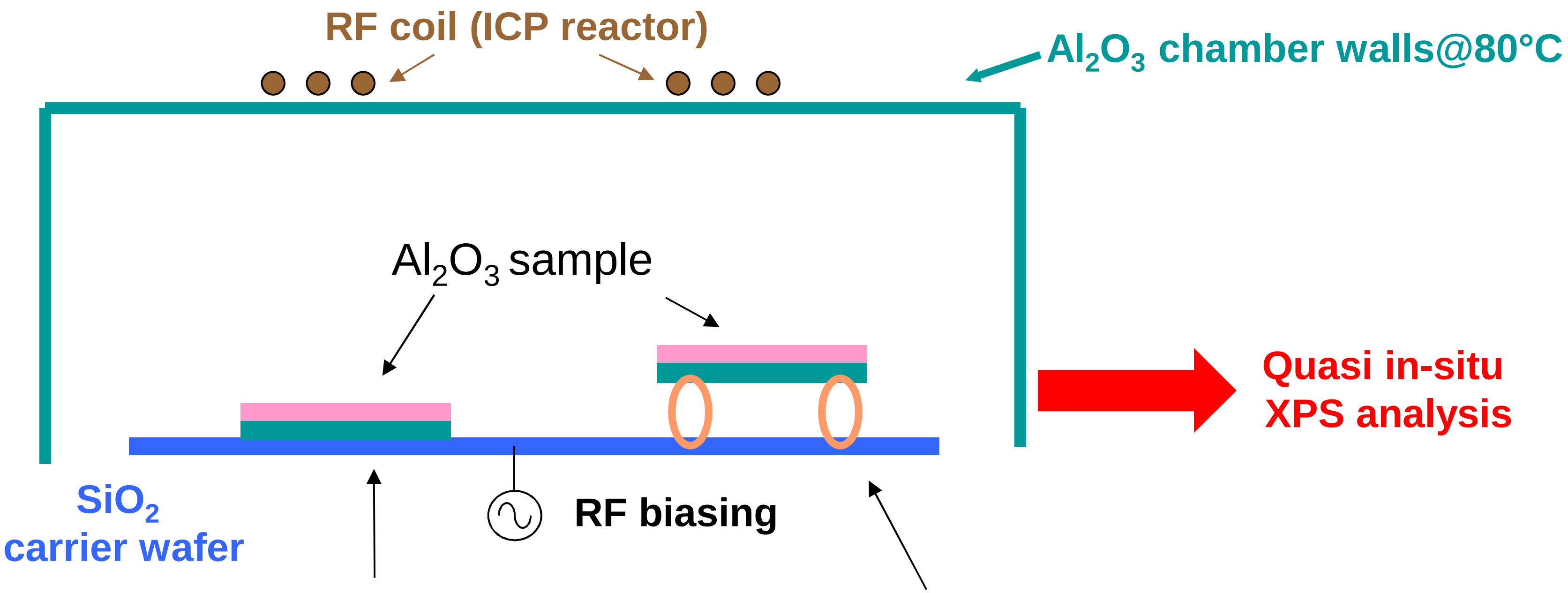
XPS
Chemical composition of the deposit formed on the Al2O3 sample

- No phosporine detected
- Deposition of a mixed SiOCl-CCl layer with encapsulated InClx residues (8%)
- No significant change after air exposure



Chamber walls cleaning strategies

Al_2O_3 sample coated with the deposit are patched on a carrier wafer and exposed to cleaning plasma in DPS



Sample patched on the carrier wafer with Fomblin:
- sample temperature regulated by ESC temperature

T between 60-90°C

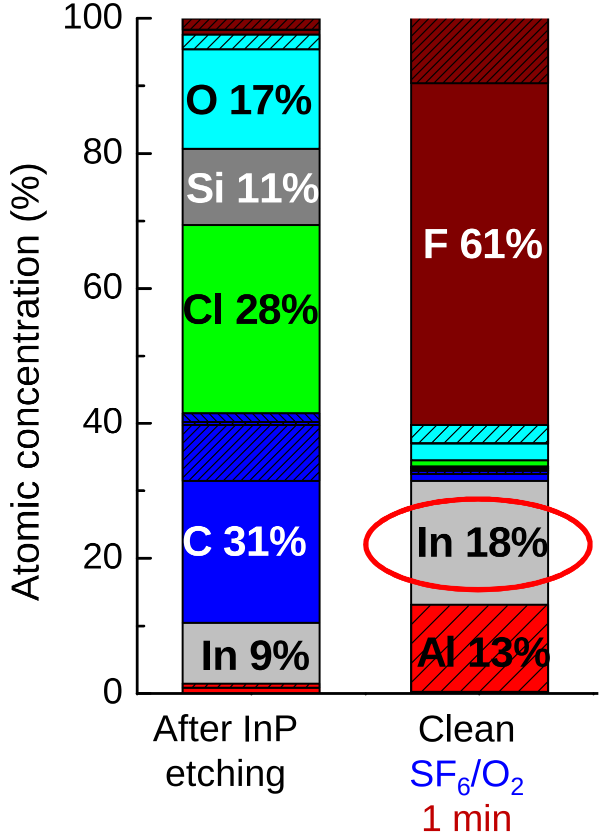
Sample elevated with Kapton rolls:
- no regulation of temperature
- temperature controlled with stickers

T >100°C

Chamber walls cleaning strategies

Preliminary tests with typical plasma cleaning strategy-Sample temperature >140°C

Gas: 100sccm
Pressure: 5-10mT
Source: 800W
Bias: 0W



- Clean SF_6/O_2: removal of SiOCCl matrix but fluorination of Al and In

Chamber walls cleaning strategies

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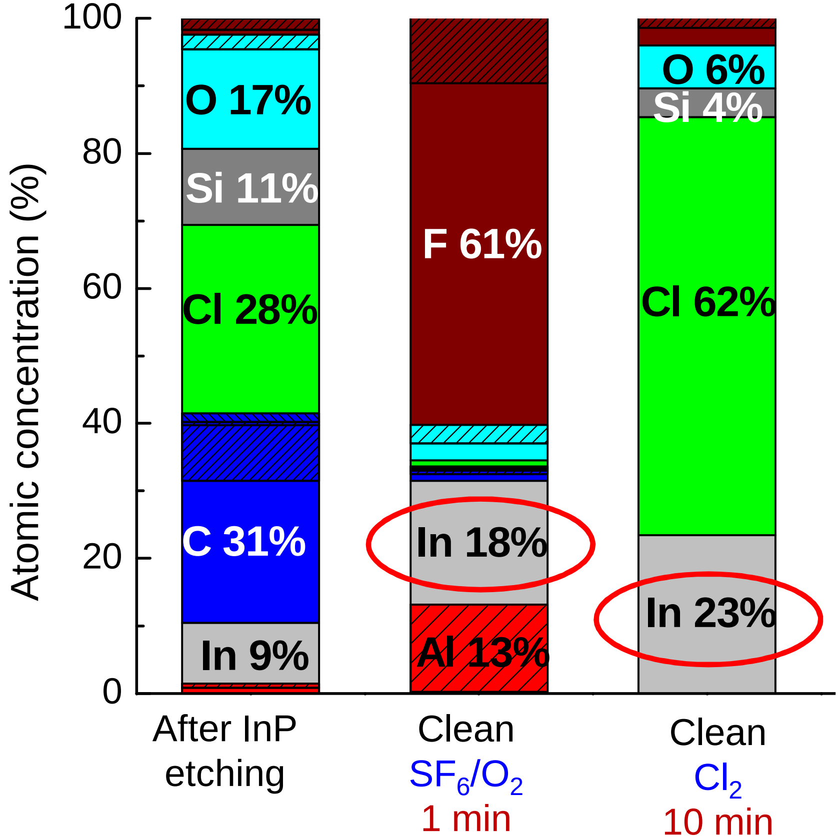

- Clean SF_6/O_2: removal of SiOCCl matrix but fluorination of Al and In
- Clean Cl_2: carbon is removed, Si slightly removed but In remains

Chamber walls cleaning strategies

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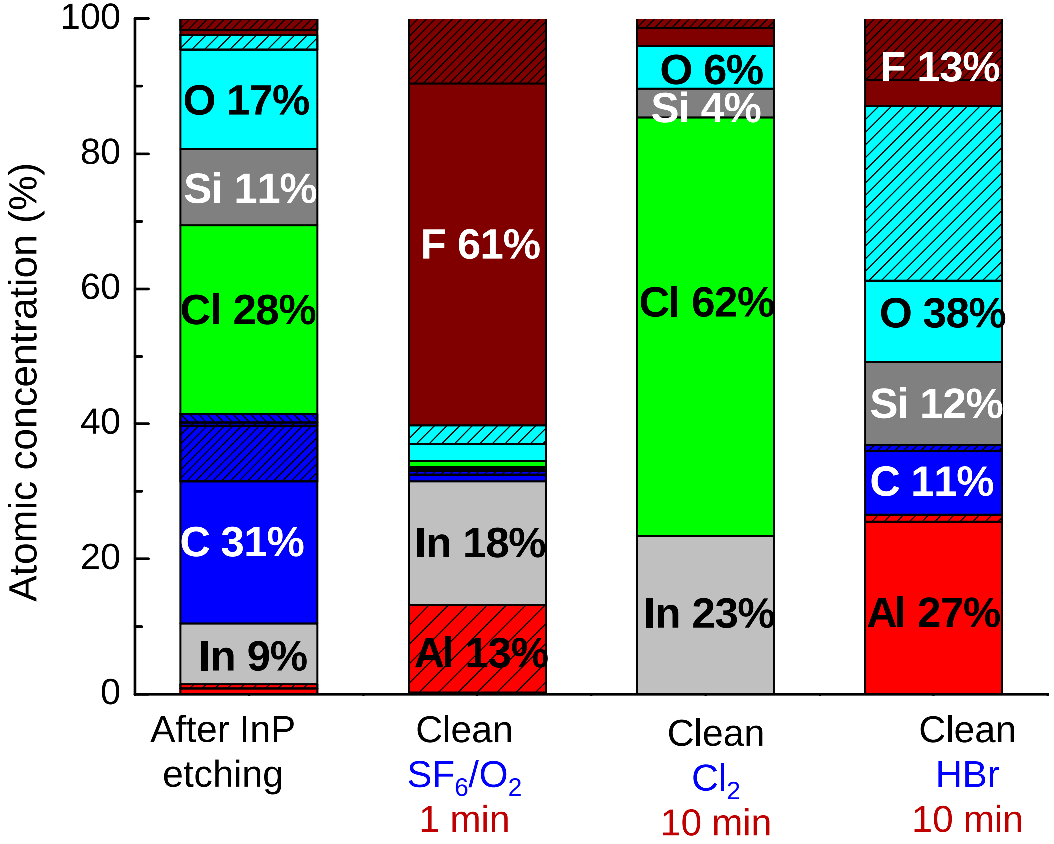
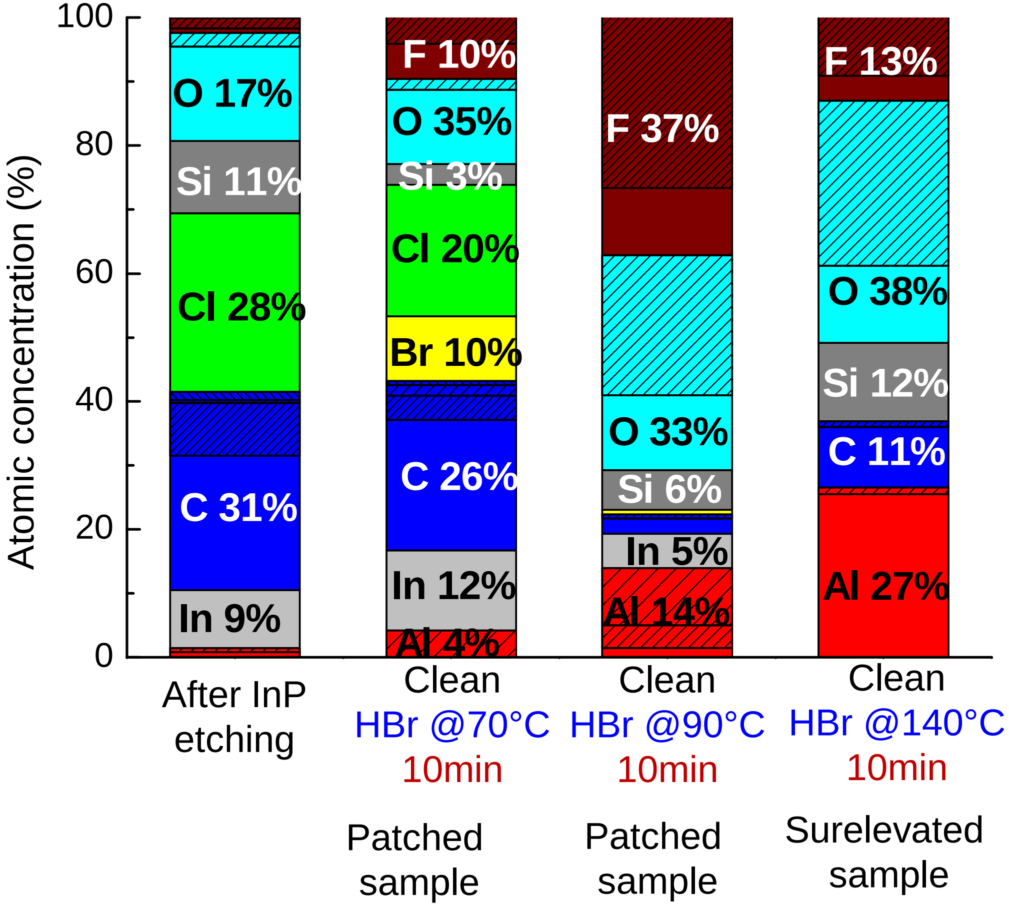
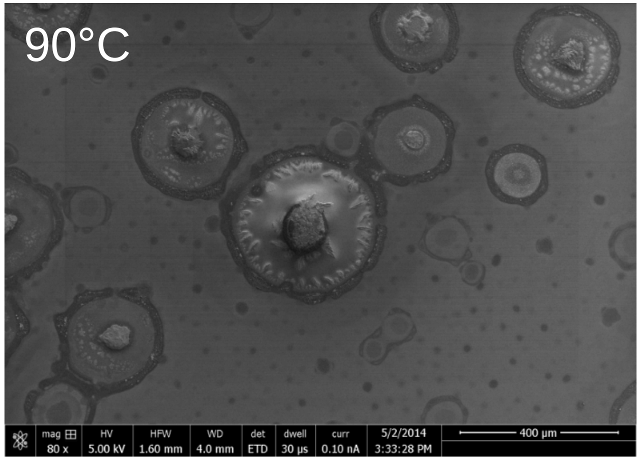
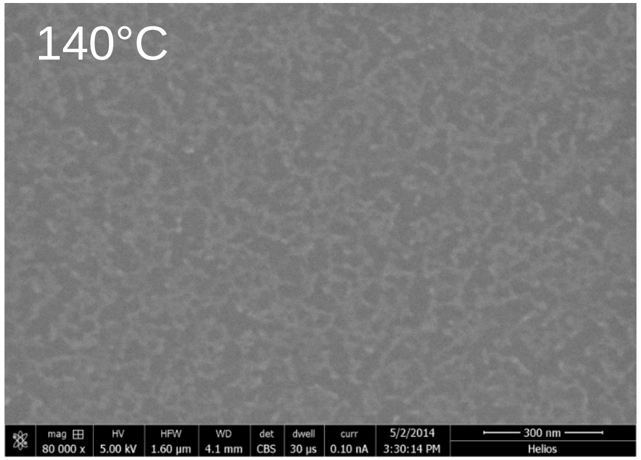


- Clean SF_6/O_2: removal of SiOCCl matrix but fluorination of Al and In
- Clean Cl_2: carbon is removed, Si slightly removed but In remains
- Clean HBr: **In is removed**

HBr plasma cleaning process: impact of temperature

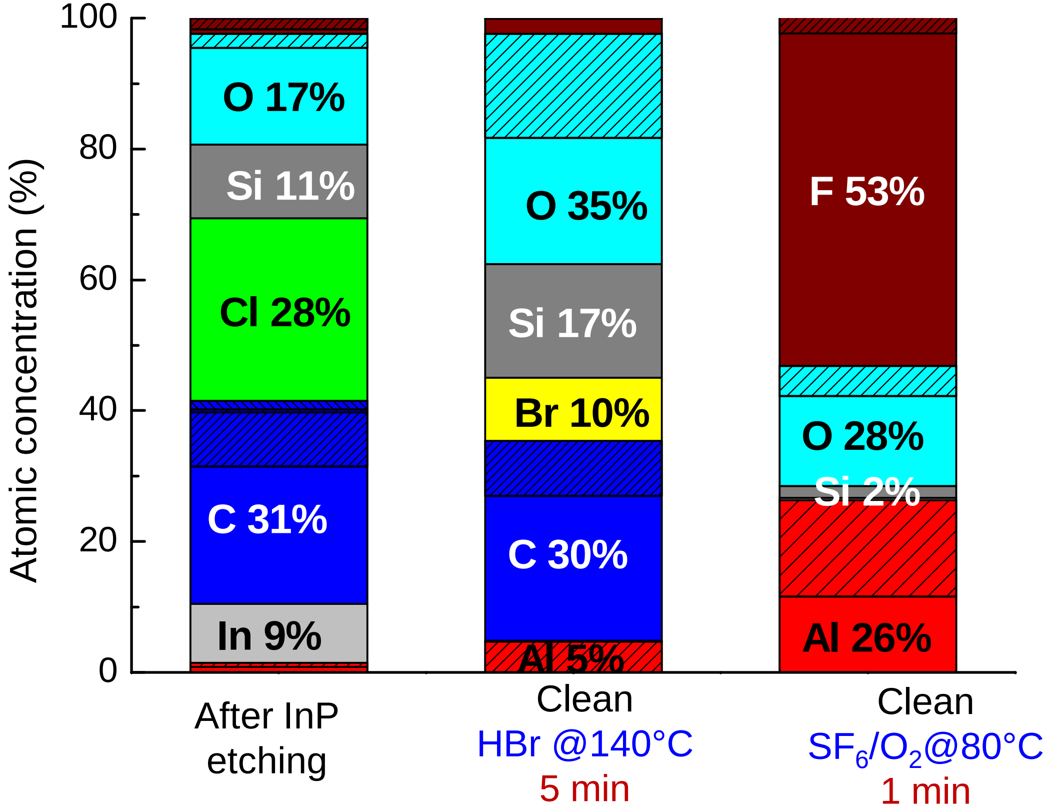






At the reactor wall temperature of 80-90°C, In residues still present

Dual step plasma cleaning process



A dual step cleaning process is efficient to restore the reactor wall:
Clean HBr@140°C remove InClx compounds followed by clean SF_6/O_2@80°C to remove Si and C based compounds

Conclusion

- Patterning of InP/InGaAs/InGaASP heterostructures can be achieved in $Ar/Cl_2/CH_4$ plasma with assistance of temperature
- During InP etching, a deposit composed of InClx residues encapsulated in a SiOCCl matrix is formed on the reactor wall.
- HBr plasma can be used to remove Indium residues from the reactor wall but for a complete efficiency, reactor wall should be heated above 100°C
- A dual step plasma cleaning process is recommended to restore the reactor wall after InP etching : HBr plasma@140°C followed by SF_6/O_2 plasma

Acknowledgement to the NANOELEC program for supporting this work

Questions?